Reduced-Transistor Full Adder Architectures for a Power-Efficient 4-Bit Array Multiplier

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Abstract:

This research uses the Cadence Virtuoso simulation environment and 90nm technology to propose a low-power 4-bit array multiplier with a modified full adder architecture. A typical array multiplier uses 28-transistor full adders to do binary addition in parallel. Nevertheless, this leads to a greater area and increased power dissipation. 22-transistor and 10-transistor full adders are used for parallel binary addition in order to solve this issue. The array multiplier with the 10-transistor full adder design uses less power and provides a better power-delay product than previous full adder designs, according to simulation data.

Keywords: power-delay product, low-power VLSI, array multiplier, full adder

I. INTRODUCTION

Multiplication is a fundamental operation used in digital signal processing systems for a number of purposes, including filtering and computing the Fast Fourier Transform (FFT). Array multipliers are used to carry out the multiplication operation in parallel, increasing the digital signal processing system's processing speed. The significant power dissipation, which is mostly caused by the high switching activity, is the multipliers' principal drawback [5].

Partial products, accumulation of partial products, and final summation are the three main steps that a multiplier typically takes to complete a particular operation. The 4-bit array multiplier is one of the most often used multipliers because of its straightforward architecture and ease of implementation, especially for VLSI design. However, conventional array multipliers make use of 28-transistor full adders, which results in increased power consumption, larger silicon area, and higher propagation delay [2].

With the increasing demand for low-power and high-performance electronic systems, optimizing arithmetic logic at the transistor level has become essential. Therefore, this work focuses on the design of a low-power 4-bit array multiplier using modified full adder logic that reduces power consumption and design complexity while maintaining reliable performance [6].

II. LITERATURE SURVEY

In reference [1], various CMOS full adder designs are analyzed using simulation tools with respect to power consumption, delay, and area. The study shows that conventional CMOS full adders provide full voltage swing and good noise margins, making them reliable for VLSI applications; however, their higher transistor count leads to increased power dissipation and larger chip area. In paper [2] low-power 1-bit full adder designs based on hybrid and transmission-gate logic are evaluated. Although these designs achieve reduced power consumption and improved efficiency, they suffer from degraded signal integrity due to operation at lower voltages. Paper [3] presents the design of a high-performance, low-power DADDA multiplier in which an optimized full adder is employed during partial product reduction to minimize the critical path delay.

In reference [4], Braun and Baugh–Wooley multipliers are implemented using QCA technology, resulting in significant reductions in power consumption and area; however, this approach is not suitable for conventional CMOS-based designs. Additionally, in paper [5], high-speed performance is achieved by combining Vedic multipliers with reversible Kogge–Stone adders, though this approach increases overall design complexity and silicon area. Similarly, reference [6], reports the use of a hybrid full adder in a Baugh–Wooley multiplier, which effectively reduces both power consumption and delay.

In reference [7], a 4×4 array multiplier based on a transmission-gate full adder is proposed, offering lower power consumption and improved speed with full-swing outputs, at the cost of a slightly higher transistor count In order to achieve the best possible balance between power and performance, Reference [8] suggests hybrid full adder-based arithmetic circuits. Nevertheless, threshold voltage loss is a disadvantage of the circuits suggested in reference [8], which may prevent the circuits from functioning at extremely low voltages. Effective parallel multiplication techniques have been suggested in reference [9] in order to reduce the reduction stages and delay time. However, for large multiplier widths, the suggested procedures in reference [9] become more difficult.

III. INTRODUCTION TO ARRAY MULTIPLIER

An array multiplier is a digital circuit designed to perform multiplication between two binary numbers. In a 4-bit array multiplier, two 4-bit inputs, A = (a_0, a_1, a_2, a_3) and B = (b_0, b_1, b_2, b_3), are multiplied to produce an 8-bit output, P = (p_0 to p_7). The creation of partial products using AND gates is the first step in the multiplication process. Full adders organized in a regular array are used to add these partial products.

The partial products can be processed and aggregated in parallel thanks to this regular array structure, which increases computation efficiency. However, the overall performance of the multiplier largely depends on the characteristics of the full adders used in its design. The logic diagram of the conventional 4-bit array multiplier considered in this work is shown in Fig. 1.

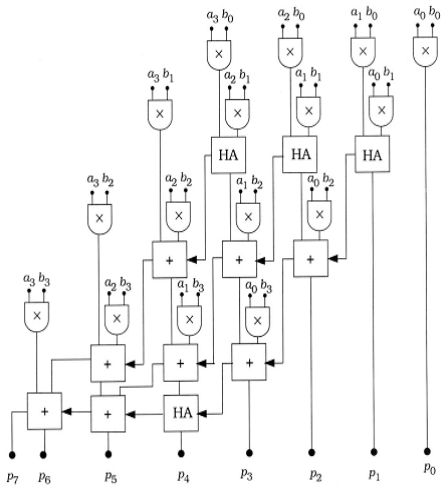

Fig. 1. Logic diagram of array multiplier.

IV. MODIFIED FULL ADDERS

A full adder is a combinational circuit used to add two input bits along with a carry input, producing sum and carry outputs. A conventional full adder typically consists of 28 transistors and provides stable and reliable output. Modified full adder designs are commonly used in complex circuits to achieve reduced power consumption and lower delay.

A. 28-Transistor Full Adder:

The 28-transistor (28T) full adder is commonly implemented using a mirror adder structure to ensure full voltage swing and reliable operation. However, the high number of transistors results in increased silicon area, which makes this design less suitable for low-power applications. The transistor-level implementation of the basic logic gates used in the 28T full adder is shown in Fig. 3.

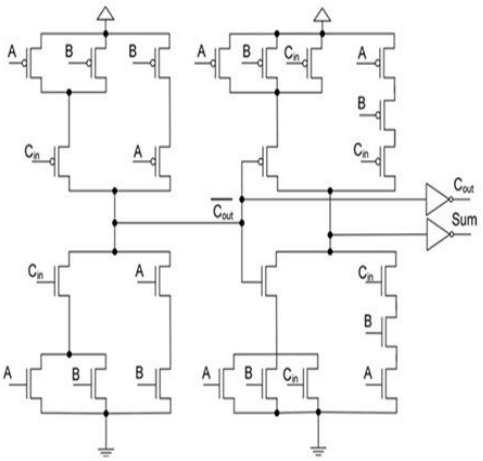

Fig. 3. Transistor level Diagrams of 28-T Full Adder

B. 22-Transistor Full Adder:

The 22-transistor (22T) full adder is based on a hybrid CMOS logic design, which offers improved power efficiency along with reliable output signal integrity.

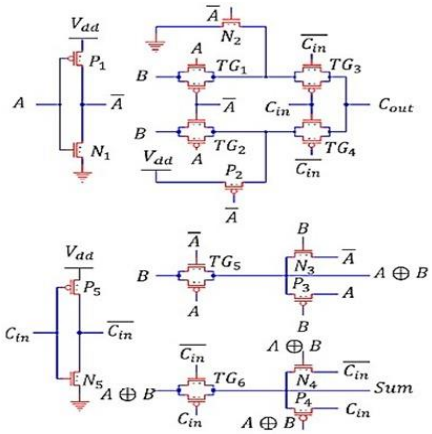

Fig. 4. 22 Transistor Full Adder

Compared to the 28T full adder, the reduced transistor count leads to lower power consumption and smaller area. The transistor-level schematic of the 22T full adder used in the array multiplier is shown in Fig. 4.

C. 10-Transistor Full Adder:

The optimized 10-transistor (10T) full adder, shown in Fig. 5, is designed using pass transistor logic to minimize the number of transistors. This approach reduces both the chip area and power consumption, but the voltage swing is compromised. Because of its straightforward design and low power consumption, the 10T complete adder circuit is regarded as effective for low-power

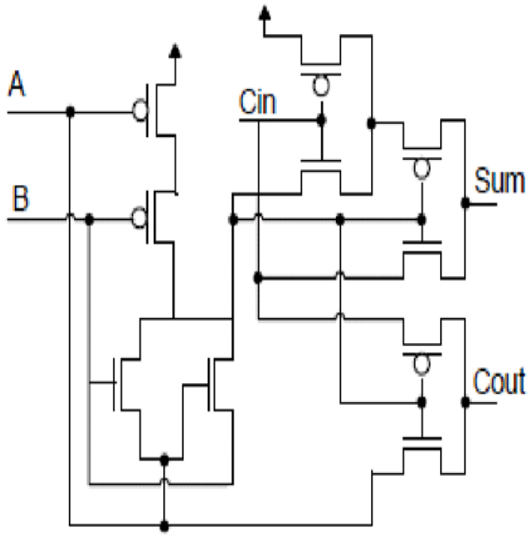

Fig. 5. 10 Transistor Full Adder

V. IMPLEMENTATION

A. Implementation of a 28T Full Adder:

A traditional VLSI arithmetic circuit using the CMOS digital logic family is the 28 transistor complete adder. To generate the sum and carry outputs with full voltage swing and robust noise margins, it uses 28 transistors. Additionally, it uses transmission gate logic and CMOS logic to guarantee the entire adder's dependability. Compared to full adder circuits designed with fewer transistors, the design is less efficient in terms of power and chip area despite the 28 transistor full adder's superior performance.

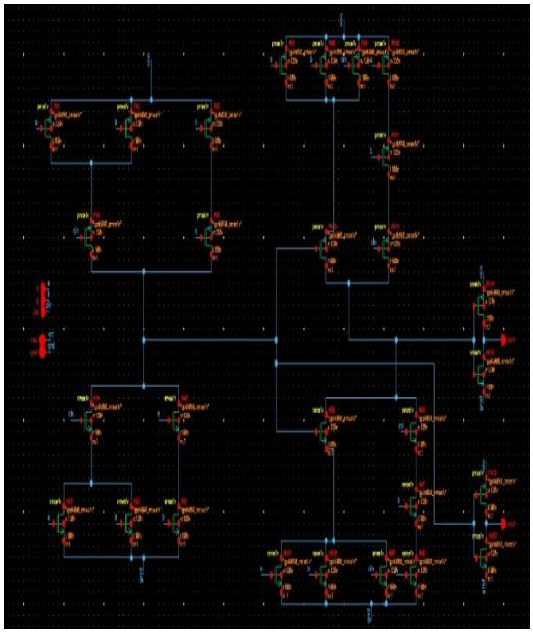

Fig. 6. 28-T Full Adder Schematic view

B. Implementation of a 22T Full Adder:

To get the Sum and Cout, three inputs—A, B, and Cin—are added using a 22-transistor (22T) complete adder. The Cadence Virtuoso tool is used to develop the 22T full adder. Fig. 6 displays the schematic of the 22T complete adder created using the Cadence Virtuoso tool.

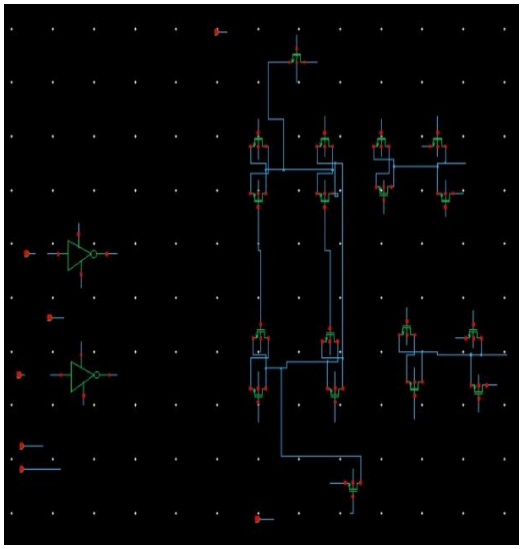

Fig. 6. 22 T full adder schematic

The schematic of the 22T full adder used in the array multiplier is shown in Fig. 6, emphasizing the proper logical connections and transistor sizing for the circuit's proper operation.

C. Implementation of a 10T Full Adder:

The pass transistor logic approach, which enables the addition of two binary integers with fewer transistors, is used to construct the 10-transistor (10T) full adder. The XOR operation is used to obtain the Sum output. $A \oplus B \oplus Cin$, whilst the reduced logic phrases are used to generate the Carry result. The Cadence Virtuoso tool is used for transistor sizing in order to ensure the designed circuit operates dependably.

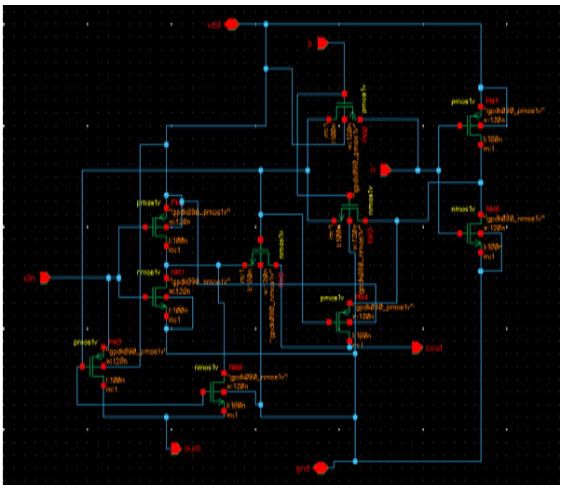

Fig. 7. 10 T full adder schematic

VI. SIMULATION AND RESULTS

Simulations of the 4-bit array multipliers based on 28T, 22T, and 10T full adders were performed using the Cadence Virtuoso tool with a 90 nm technology library under identical operating conditions. These simulations verify the correct functional operation of the multipliers in terms of their multiplication capability.

Key performance parameters such as power consumption, propagation delay, and power–delay product (PDP) were extracted and analyzed for comparison. Additionally, it can be seen that, although having the lowest propagation delay of all the compared architectures, the array multiplier built with the 28T full adder exhibits the highest power usage. The 22T full adder–based multiplier shows comparable delay with reduced power consumption. Among all designs, the 10T full adder–based multiplier achieves the lowest power consumption and power–delay product, with an acceptable increase in delay.

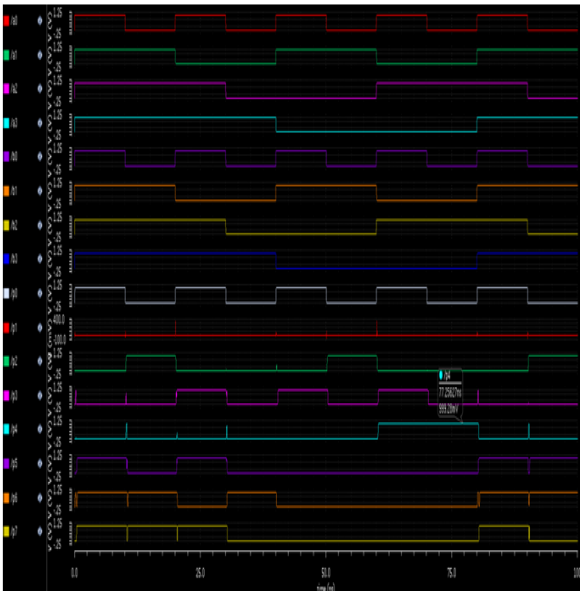

Fig. 8. Output of 28T FA based Array multiplier

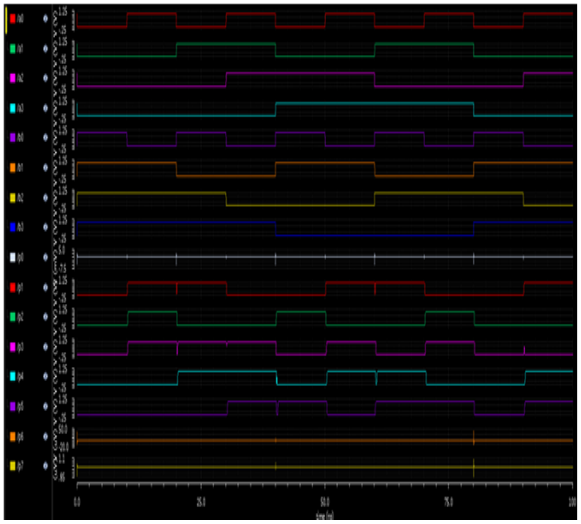

Fig. 9. Output of 22T FA based Array multiplier

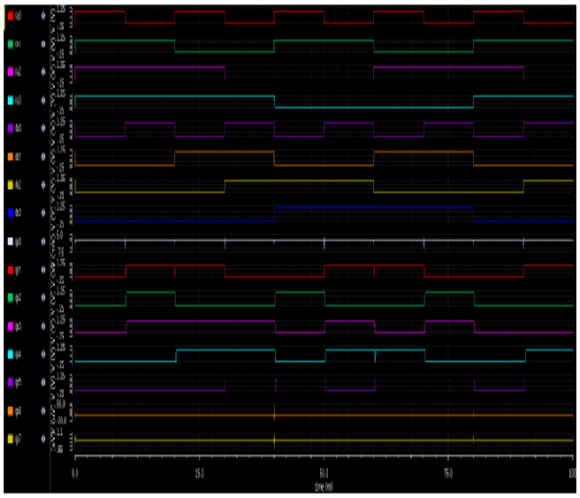

Fig. 10. Output of 10T FA based Array multiplier

Fig. 8 shows the simulated output waveform of the 4-bit array multiplier implemented using a 28T full adder. The output waveform of the 22T full adder–based array multiplier is presented in Fig. 9. Fig. 10 illustrates the output waveform of the 10T full adder–based array multiplier, confirming correct operation.

Table 1 presents a comparative performance analysis of the 4-bit array multipliers implemented using 28T, 22T, and 10T full adder architectures. The comparison is based on power consumption, propagation delay, and PDP values obtained from Cadence Virtuoso simulations at the 90 nm technology node under the same operating conditions.

Table 1. Comparison table

	28-T Conventional adder based 4-bit array multiplier	22-T Hybrid adder based 4-bit array multiplier	10-T Conventional adder based 4-bit array multiplier
Delay	30.2991 ps	30.338 ps	34.6226 ps
Average power	8.27996 uw	5.83587 uW	4.69264 uW
PDP	250.875 fWs	177.052 fWs	162.453 fWs

With a delay that remains comparable, the 10T-based design demonstrates significantly lower power consumption. As a result, the 10T full adder–based multiplier emerges as the most energy-efficient option, exhibiting the lowest power dissipation and power–delay product while maintaining similar latency.

VI. CONCLUSION

This work presents the design and comparative analysis of 4-bit array multipliers implemented using 28T, 22T, and 10T full adder architectures in a 90 nm technology process. The array multiplier built with the 10T full adder exhibits superior energy efficiency with comparable propagation latency, as can also be seen from the simulation results. These findings support the idea that array multipliers with compact, low-power complete adders, such as the 10T, are better suited for low-power VLSI applications. However, because there is less voltage fluctuation, these architectures may still have limits even with relatively few transistors. Overall, this study demonstrates that circuit-level optimization plays a significant role in enhancing the performance of VLSI systems.

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