Mixed Mode S-Parameter Analysis of Multilayered Differential Via for Signal Integrity

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***Abstract*— Vias act as the major source for the signal attenuation in high-speed digital design. At high data-rates, interconnect path impedance must be uniform to avoid signal attenuation. But, various factors like data-rates, Via geometry, line terminations etc. contribute to change of line impedance. Basically, line impedance can be controlled with ease, but it is difficult to maintain uniform impedance for a Via geometry. It is prerequisite to design, validate and optimize the differential Via geometry. Accordingly, techniques like controlled impedance line design (CILD) are necessary to ensure Via offers uniform impedance to avoid signal attenuation. Here, a parameterized differential Via geometry is designed with two approaches i.e., stub length and back-drill. Further, differential Via is characterized in frequency domain with mixed mode S-parameters using a full 3-D finite element method (FEM) simulator. Mixed mode S-parameters results substantiate that differential Via with stub length offers low impedance Zc = 67.54 Ω, high return loss S_{11}=-10.78 dB, S_{21} = -0.494 dB. Whereas differential Via designed with back-drill approach offers high impedance Zc = 96.13 Ω, low return loss S_{11}=-28.82 dB, S_{21} = -0.0444 dB. Therefore, the proposed back-drill approach offers better Via impedance matching than the stub length**.

Keywords*— *Interconnect, Return loss, Insertion loss, Via, Back-drill, Controlled Impedance Line Design, Back-drill, Printed Circuit Board, Giga-hertz, Finite Element Method, Signal Integrity, TDR Analysis, S-parameters.

I. INTRODUCTION

In high-speed digital designs, the rate of data transmission has drastically increased from 28 Gbps to 56 Gbps. Applications such as PCIe, DDR3, DDR4 SD-RAM, USB etc. have the clock frequencies which are running at several giga-hertz (GHz) [1]. Further, signal-edge-rates have increased drastically with signal frequencies. In order to handle, these increased data-rate signals, multi-layer routed printed circuit boards (PCB) are necessary. Also, electro-magnetic compatibility (EMC) and Signal Integrity (SI) issues have prime impact on performance and quality of the signal respectively. Invariably, the primary challenge on a high density multi-layered integrated circuit (IC) or PCB is routing. More often, Via's in a multi-layer PCB stackup [2] are used to route several levels of signal layers for the signal propagation. In high-speed design, Via transition and a transmission line or interconnect forms the *interconnect trace/path* which handles and allows signal data-rates of Gbps. During signal transition, Thru and short Vias act as the major source for the signal attenuation. Therefore, Vias leads to the issues of signal integrity (SI) and electro-magnetic compatibility (EMC) [3], [11]. These issues have become more complex and are challenging in multi-layer design process. Most of the transmission lines used in high-speed designs often uses differential signaling with line impedance Z_C=100 Ω instead of a single-ended signaling. The transmission interconnect path is designed such that, the single-ended or differential line impedance exhibit uniform through-out; even for changing signal frequencies. However, it is important to understand the characteristic behavior of line impedances for changing data-rates, geometry etc. to avoid signal losses. The input-output performance of differential high-speed interconnect path can be maximized with uniform impedance. In high-speed designs, transmission line impedance can be controlled with ease by varying the width of the line. Moreover, line impedance is based on; applied input signals, line separation, line matching etc. Physical design of Via geometry with impedance equal to differential transmission line is highly difficult. So, it becomes difficult to control the Via impedance and majority of the signal attenuation is primarily due to Via. In a multi-layer PCB stack-up [12] the signal has to route through many signal layers and through different Via's. as well. In a typical integrated circuit (IC), printed circuit board (PCB) boards and packages; Via's have impedance discontinuities because each signal layer has different impedances that leads to signal attenuation.

II. RELATED WORK ON MULTI-LAYER

In a multi-layer PCB stackup, IC and packages [4] often the data-rates are in Gbps. The signal has to propagate through several layers and also through different Via; that are electrically short in length. Signal degradations 70-80%. is primarily because of Via's geometry. In-order to avoid the resonance effects in PCB Via's; designers primarily focus on maximum allowable stub length for Via design. Therefore, new approaches for the design of parameterized Via structure

is important to ensure appropriate uniform line impedance is offered and also the signal losses are nullified.

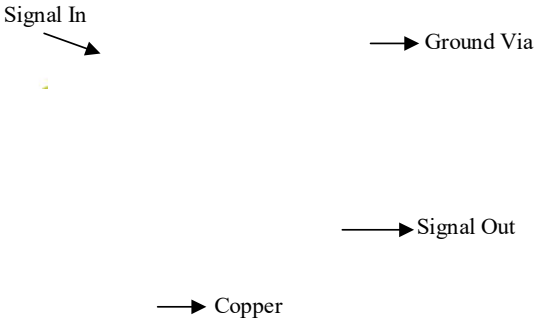


Fig. 1. Multi-layer PCB Stack-up with Signal Planes.

A typical high-speed multi-layer PCB stack-up with differential Via and stub length is shown in Fig.1. Most of the high-sped designs uses differential signaling instead of single-ended signaling. Any general methodology could be adopted for design of differential Via based on stub length.

A.Kavitha et al. [5] have proposed a Via optimization method along with TDR analysis to achieve minimum crosstalk by using single-ended S-parameters. Effects like surface roughness and insertion loss (S_{11}) of differential Via were evaluated. The characterization of Via was limited to single-ended mode. Mixed mode characterization of differential Via was not performed.

Yu Yang Deng et al. [6], designed a 3-D model of differential Via. Here, optimization of a differential Via was performed based on the stublength. S-parameters was used for the characterization of differential Via.

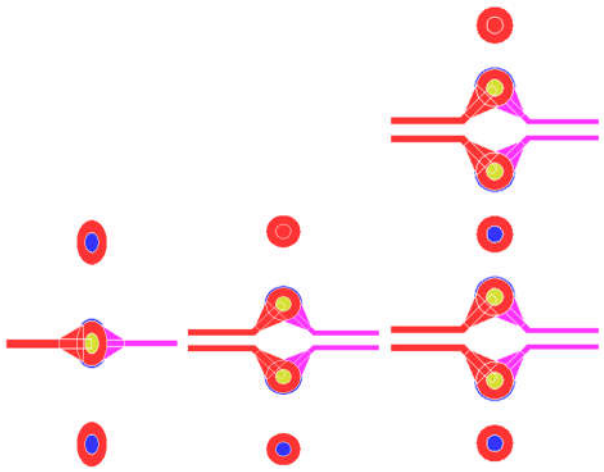
Andreas Hardock et al. [7] have proposed a method to design a single-ended geometrical structure of Via. Investigated the performance of Via in frequency domain. Further, elaborated the method to control the impedance of single-ended interconnect path. However, approach for the design of differential Via, differential transmission line and method to control impedance were not discussed.

Armen Vardapetyan et al. [8] primarily focused on techniques for optimization of high-speed differential Via on circuit boards that are signaling at high data-rates. Here, only Via optimization process to reduce the signal degradation was discussed but not about differential Via impedance control methods.

Junda Wang et al. [9] have designed the differential Via geometry for the reduction of crosstalk in high-speed PCB's. A tilted drilling approach was used to mitigate the crosstalk noise. Line impedance control method was not presented.

III. Multi-Layer Via Modeling

In a multi-layer PCB geometry, often high-speed signal has to propagate through limited cross-sectional area of Via. Therefore, to avoid the electromagnetic radiation and crosstalk PCB components are placed on the top layer. Whereas, in differential lines signal propagation is in the inner layers of multi-layer. Vias are necessary to connect components (top layer) and the inner signal layers.



a) Single-ended Via b) Differential Via c) Arrays of Via

Fig. 2. Different Types of Multi-layer Via.

During signal switching, Via can cause impedance discontinuity when high data-rate signal propagates through which results in un-desired signal reflections. Also, Via allows the high date-rate signals to propagate through many levels of signal layers. Different types of Via's are used in multi-layer substrate i.e., blind, buried, thru (barrel) respectively. A cross-sectional view of various types of Via's is shown in Fig.2. Based on the application, Via's are classified as single-ended, differential and array of Via.

A 3-dimensional differential Via [9] geometry mounted with a teardrop is shown in Fig.3. Microstrip line is a signal layer on top and stripline is the signal layer at the bottom of stackup. A signal Via is often used between layers for signal transition. Pad connects signal line and a Via. Ground Via connects the return current of high-speed signals. Anti-pad controls the spacing between Via and copper to avoid electrical short. In a multi-layer structure, pads which don't connect to signal lines are termed as non-functional pads (NFP).

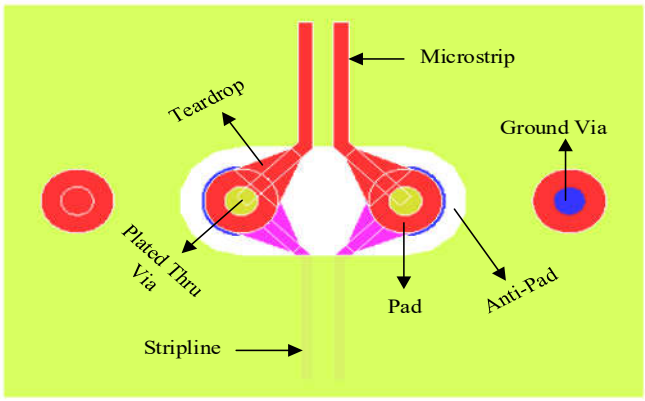


Fig. 3. Multi-layer Stack-up with Blind and Thru Via's.

A multi-layer PCB stackup which is designed with high-speed material Megtron as substrate with dielectric constant of $\varepsilon_r = 3.4$. It has a loss-tangent of δ=0.02. An optimized

differential Via designed with parameters as given in [5], is listed in Table 1.

TABLE I. RANGE OF DIFFERENTIAL VIA PARAMETERS [5]

Via Parameters	Min Value (mils)	Max Value (mils)
Via diameter	8	12
Pad diameter	18	22
Anti-pad diameter	30	32
Separation between Via	40	40
Via pitch	30	36

IV. DESIGN OF MULTI-LAYER DIFFERENTIAL VIA

This section details the approaches that are necessary to design a high-speed differential Via in a multi-layer substrate. The fundamental design parameters to design any Via are: substrate stack-up, Via designed with proper impedance. Preferably, differential signaling scheme is used for signal transition with a differential line impedance of Zc=100 Ω. Figure 4 shows a multi-layer PCB substrate designed with 16 signal layers [5] for differential Via analysis. A plated Thru hole (barrel) Via connects all the signal layers in the substrate. The layers on the substrate are defined as signal layers, ground planes (return path) respectively.

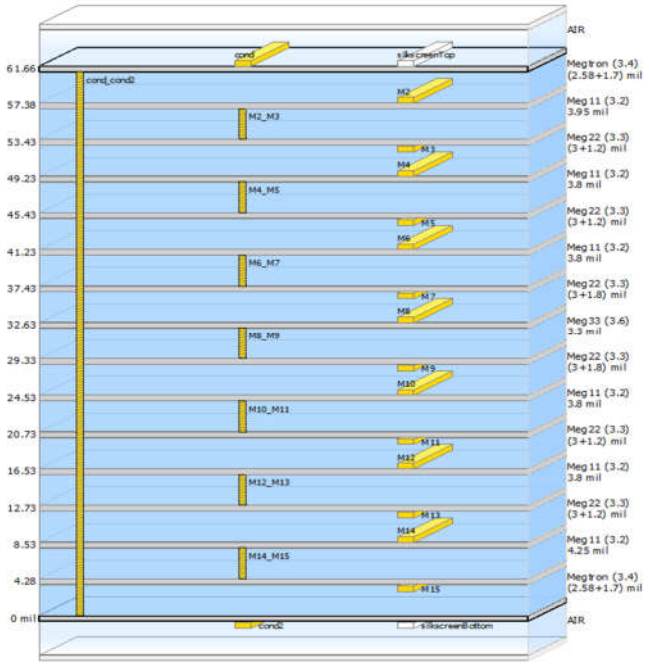


Fig. 4. Multi-layer Stackup Design with Thru and Blind Via's.

In a multi-layer PCB stackup, microstrip and striplines [15], [16] are fundamental components that are widely used as conductors for signal transmission. As shown in Fig.4, on top of a substrate (cond) edge coupled microstrip line is a conductor; layer M2 as its ground plane for return current. Similarly, an edge-coupled stripline is at layer M5 as another conductor; layers M4, M6 as its ground plane. In the design of multi-layer PCB substrate; Controlled Impedance Line Design (CILD) feature is used. This feature is used to obtain optimally synthesized microstrip and striplines with specific uniform differential line impedance of 100 Ω. An optimized edge-coupled microstrip line designed with CILD feature at 10 GHz frequency has design parameters: length = 100 mil, width = 3.797 mil, spacing = 5 mil. The design parameters of stripline are: length = 10-inch, width = 2.9408 mil, spacing = 5 mil.

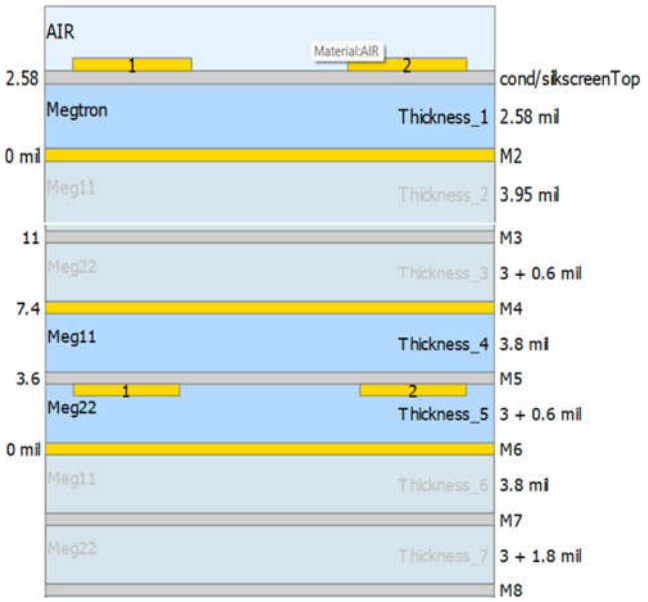


Fig. 5. Edge-Coupled Microstrip and Striplines on Substrate.

V. ANALYSIS OF MULTI-LAYER DIFFERENTIAL VIA

S-parameter characterization and analysis of a multi-layer differential Via i.e., both single-ended and mixed mode [11], is performed in frequency domain. From the analysis, performance metrics such as inductance offered by Via, return loss (S_{11}), insertion loss (S_{21}) are evaluated.

A. Single-Ended Analysis of Differential Via

At high frequencies, S-parameters are best suited and are widely used for characterization of device behavior in frequency domain. S-parameters [13] allows to analyze the complex device behavior easily and predicts device response accurately. The single-ended S-parameter represent device characterization with only one input port exited with stimulus and other ports are terminated. A differential Via yields a scattering matrix with 16 element measurements. The single-ended differential Via properties such as Z0, NEXT, FEXT, phase delay can be evaluated using the S-parameters [14] as given in equation (1).

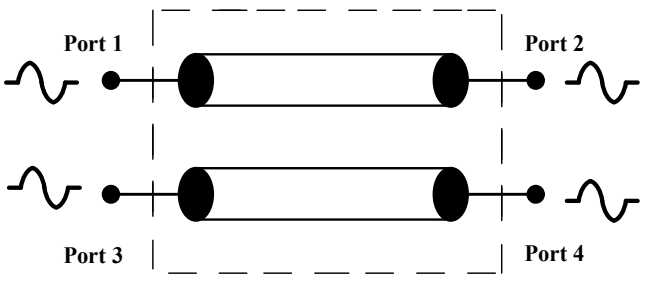
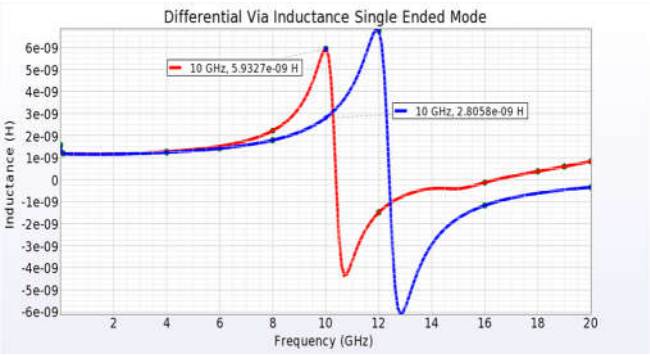


Fig. 6. Differential Pair Single-Ended Mode Analysis.

$$S_{std} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \quad (1)$$



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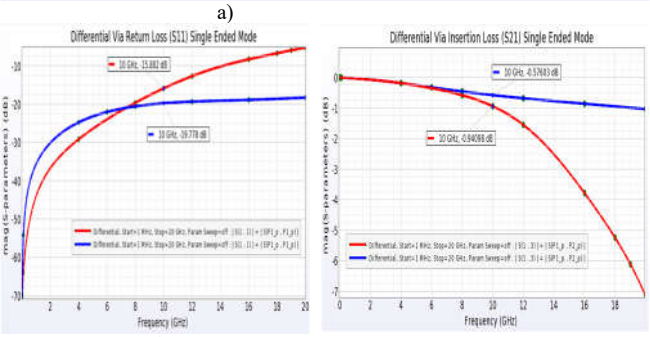


b) c)

Fig. 7. a) Inductance with stublength and backdrill. b) Return loss (S_{11}) of Via c) Insertion loss (S_{21}) of Differential Via.

The differential Via geometry performance is characterized with both stub length and back-drill [16] approaches respectively. A single-ended S-parameter analysis of differential Via is performed using 3-D FEM simulator from 1 MHz to 20 GHz in frequency domain. Figure 6(a) shows the response of inductance offered by differential Via. At mid frequency 10 GHz, Via with stub length has inductance L=5.932nH; with back-drill inductance lowered to L=2.805nH. As shown in Figure 6(b), differential Via return loss is S_{11}=-15.882 dB. It is quite high when compared with back-drill approach S_{11}=-19.778 dB. The decrease of Via inductance has decreased return loss (S_{11}) and increased the insertion loss (S_{21}) which is primary for efficient signal transmission.

Similarly, Figure 6(c), shows the single-ended insertion loss or forward gain (S_{21}) offered by differential Via with stub length and back-drill approaches. The forward gain because of back-drill approach is S_{21}=-0.94098 dB while with stub length is S_{21}=-0.57603 dB.

B. Mixed Mode Analysis of Differential Via

In a high-speed multi-layer design, often differential signaling are used widely for broad band applications. Evaluation of these differential lines are essential for optimal circuit performance. Mostly, single-ended S-parameter analysis ignore the effects of coupling between the signal layers at high frequencies. An alternate method is to use mixed mode S-parameters [12], [14] that are suited for differential line characterization.

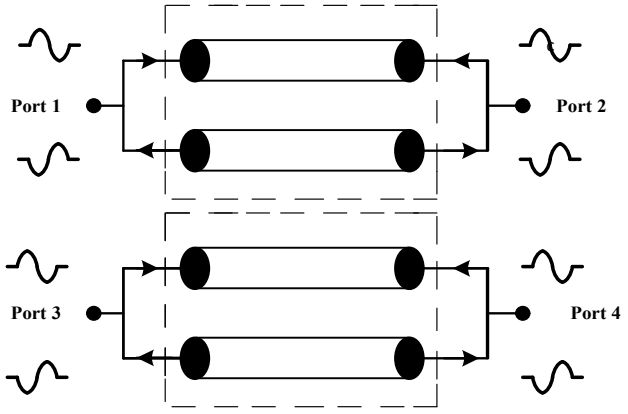


Fig. 8. Differential Pair Mixed Mode S-parameter Analysis.

Mixed mode analysis reports differential and common mode of operation for coupled layers. The transformation of single-ended S-parameters to mixed mode S-parameters is given in following equations.

$$\begin{bmatrix} S_{DD} & S_{DC} \\ S_{CD} & S_{CC} \end{bmatrix} \quad <=> \quad \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \tag{2}$$

$$S^{mm} = MS^{std}M^{-1} \tag{3}$$

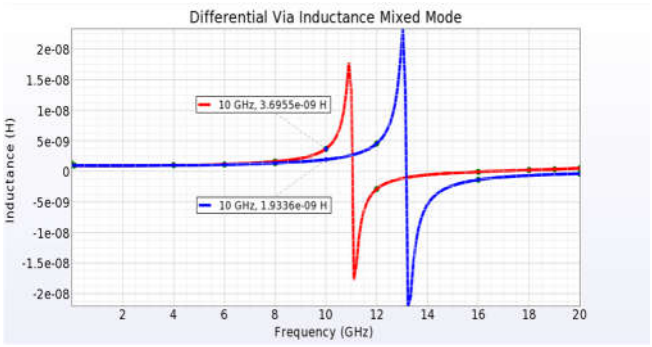
$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} S_{DD} & S_{DC} \\ S_{CD} & S_{CC} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} \begin{bmatrix} S_{11}-S_{12}-S_{21}+S_{22} & S_{13}-S_{14}-S_{23}+S_{24} \\ S_{31}-S_{32}-S_{41}+S_{42} & S_{33}-S_{34}-S_{43}+S_{44} \end{bmatrix} \begin{bmatrix} S_{11}+S_{12}-S_{21}-S_{22} & S_{13}+S_{14}-S_{23}-S_{24} \\ S_{31}+S_{32}-S_{41}-S_{42} & S_{33}+S_{34}-S_{43}-S_{44} \end{bmatrix} \\ \begin{bmatrix} S_{11}-S_{12}+S_{21}-S_{22} & S_{13}-S_{14}+S_{23}-S_{24} \\ S_{31}-S_{32}+S_{41}-S_{42} & S_{33}-S_{34}+S_{43}-S_{44} \end{bmatrix} \begin{bmatrix} S_{11}+S_{12}+S_{21}+S_{22} & S_{13}+S_{14}+S_{23}+S_{24} \\ S_{31}+S_{32}+S_{41}+S_{42} & S_{33}+S_{34}+S_{43}+S_{44} \end{bmatrix} \end{bmatrix}$$

After the transformation, the overall mixed mode S-parameters of a differential pair which is derived from the above equations yields Smm.

$$S_{mm} = \begin{bmatrix} \begin{bmatrix} S_{DD11} & S_{DD12} \\ S_{DD21} & S_{DD22} \end{bmatrix} \begin{bmatrix} S_{DC11} & S_{DC12} \\ S_{DC21} & S_{DC22} \end{bmatrix} \\ \begin{bmatrix} S_{CD11} & S_{CD12} \\ S_{CD21} & S_{CD22} \end{bmatrix} \begin{bmatrix} S_{CC11} & S_{CC12} \\ S_{CC21} & S_{CC22} \end{bmatrix} \end{bmatrix} \tag{5}$$

The mixed mode S-parameter analysis of a differential Via geometry designed with both stub length and back-drill approaches is performed from 1 MHz to 20 GHz. Figure 9 shows the simulation response of inductance, return loss (S_{11}) and insertion loss (S_{21}) offered by differential Via using mixed mode analysis.



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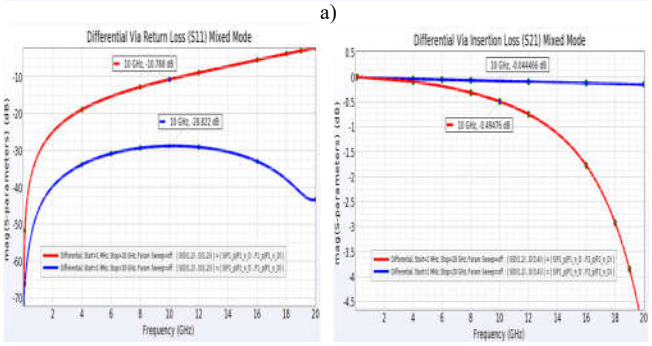


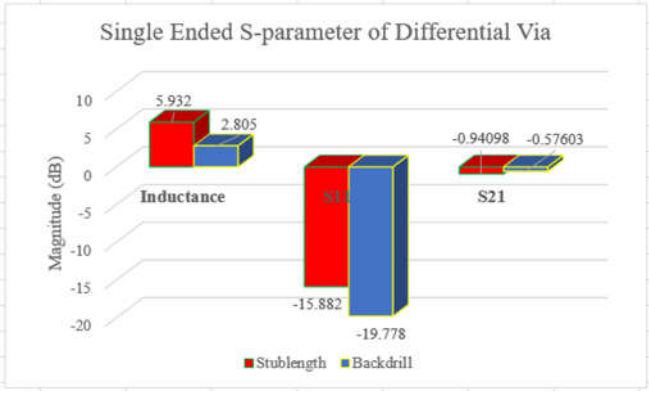
b) c)

Fig. 9. a) Inductance with stublength and backdrill. b) Return loss (S11) of Via c) Insertion loss (S21) of Differential Via.

TABLE II. PERFORMANCE OF DIFFERENTIAL VIA WITH MODES

Mode of Analysis	Approach for Via	Inductance (nH)	Return loss (S_{11}) dB	Insertion loss (S_{21}) dB
Single-ended [5]	Stublength	5.932	-15.882	-0.94098
	Backdrill	2.805	-19.778	-0.57603
Mixed Mode [Proposed]	Stublength	3.699	-10.788	-0.49476
	Backdrill	1.993	-28.882	-0.04446

Table II list the performance metrics of a differential Via designed with stub length and back-drill approaches evaluated using both single ended and mixed mode analysis. The metrics in table shows that differential Via designed with back-drill has offered better performance than with stub length. Also, a comparison of single-ended and mixed mode S-parameters is shown in Fig.10.



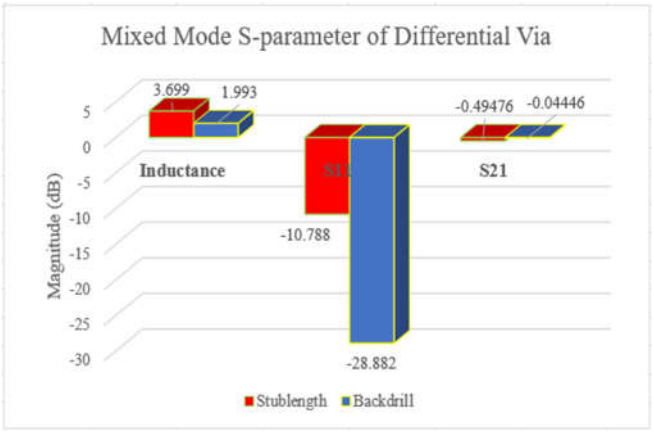


Fig. 10. Comparison of Single-ended and Mixed Mode Via Performance.

VI. TDR ANALYSIS OF VIA FOR IMPEDANCE

In high-speed digital design; time domain reflectometry (TDR) analysis is preliminarily conducted to know about the impedance discontinuities in a differential line. A single-ended mode TDR [10] analysis of differential Via with stub length is performed to evaluate differential impedance offered by Via. Simulation response shows the maximum impedance offered by differential Via with stub length which is quite low i.e., Zc = 40.564 Ω.

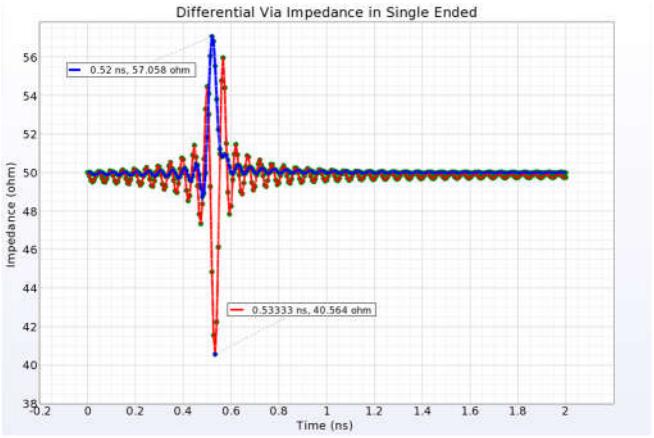


Fig. 11. Impedance of Via using Single ended TDR.

At high frequency, low impedance yields high return loss(S_{11}) because of impedance mismatch. Line impedance improvement can be achieved in various ways. Via back-drill approach can be used to enhance performance and differential impedance Zc = 100 Ω approximately. In Via back-drill approach, total length of stub = 45.22 mil is reduced gradually by stub =2 mil from bottom to top of differential Via. Back-drill approach design reduces the effect of stub on Via thereby increases the S_{21} and also increases the impedance to Zc =57.058 Ω as shown in Fig.11.

Similarly, mixed mode TDR analysis of differential Via is performed and response is shown in Fig.12. Differential impedance of Via with stub length is 67.541 Ω and with back-drill approach is 96.133 Ω. Further, result shows that back-drill approach enhances the insertion loss (S_{21}) and decreases the return loss (S_{11}).

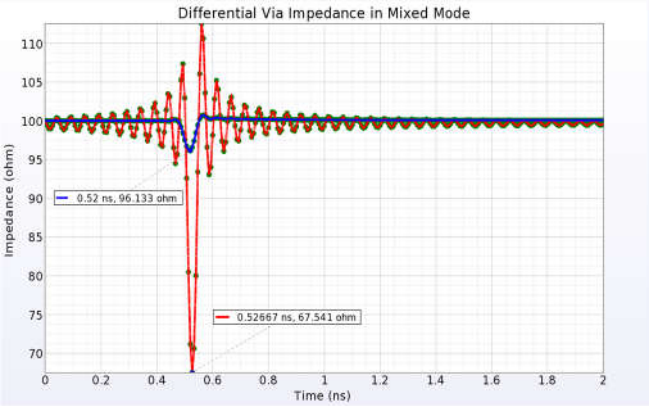


Fig. 12. Impedance of Via using Mixed mode TDR.

The differential Via impedance evaluated with single-ended and mixed mode time domain reflectometry analysis designed with stub length and back-drill approaches is listed in Table III.

TABLE III. IMPEDANCE OF DIFFERENTIAL VIA

Mode of Analysis	Approach for Via	Differential Impedance (Ω)
Single-ended [5]	Stublength	40.564
	Backdrill	57.058
Mixed Mode [Proposed]	Stublength	67.541
	Backdrill	96.133

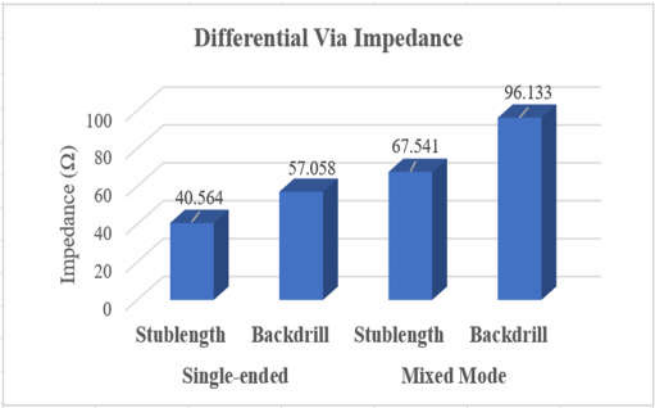


Fig. 13. Impedance of Via using Mixed mode TDR.

As shown in Fig.13, the impedance offered by a differential Via must be equal to line impedance i.e., Zc=100 Ω. Mixed mode analysis of differential Via with back-drill has offered an impedance 96.133 Ω. The impedance offered by single-ended back-drill is 57.058 Ω which very for low for differential signaling. It leads to increase of return loss (S_{11}) because of impedance mismatch.

VII. CONCLUSION

In high-speed digital designs, often multi-layer stackup's are used for regular signal transitions between differential signal lines and differential Vias. Multi-layers are necessary to reduce the impedance mismatch. Impedance discontinuity causes reflections and leads to signal integrity problems. This paper presents a modelling of differential Vias designed with stub length and back-drill approaches. A differential Via on a 16-layer PCB is analyzed using single ended and mixed mode S-parameters in frequency domain. Firstly, Via stub length causes deep effect on impedance with higher frequency points and results in a degradation of the differential Via performance. The Via stub length effect leads to impedance mismatch and also leads to increase of S_{11} and decrease of S_{21}. TDR analysis of differential Via showed a uniform impedance of 96.13Ω was achieved using proposed back-drill approach. Inductance effect at high frequencies also got reduced to 1.933nH because of back-drill approach. At 10 GHz frequency, mixed mode S-parameter shows that return loss has decreased S_{11} = -28.882 dB and insertion loss has also increased S_{21} = -0.0446 dB because of back-drill. The analysis and simulation metrics shows that differential Via designed with back-drill has offered better performance than with stub length. Additionally, ground Via's can be placed near the signal Vias which will further help to improve the performance at high frequencies.

REFERENCES

[1] Ben Toby, "Rapid Design of High Performance 25+ GT/s Vias by Application of Decomposition and Image Impedance" , Signal Integrity Journal, 4-May 2017.

[2] Kai-Bin W, Lin C-Y, Huang S-Y, Ruey-Beei W "Design of Stackup and Shorting Vias and for Reducing Edge Radiation in Multilayer PCB" Proceedings of IEEE Electrical Design of Packaging and Systems Symposium, 2016.

[3] Fan, J.; Ye, X.; Kim, J.; Archambeault, B.; Orlandi, A. Signal Integrity Design for High-Speed Digital Circuits: Progress and Directions. IEEE Trans. Electromagn. Compat. 2010, 52, 392–400.

[4] C. S. S. Rao, S. Tunga and A. K. G, "Analysis of high speed design on a multilayer PCB substrate," 2021 International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT), Bangalore, India, 2021, pp. 713-717.

[5] A.Kavitha, Ch. Sekhararao Kaitepalli, J. N. Swaminathan, "16- Layer PCB Channel Design with Minimum Crosstalk and Optimization of VIA and TDR Analysis", Journal of Electronic Testing, Springer, 2019.

[6] Y. Deng, Z. Li, Y. Yu, B. Li, X. Wang and Z. Wu, "S Parameters Optimization of High-Speed Differential Vias Model on A Multilayer PCB," 2022 23rd International Conference on Electronic Packaging Technology (ICEPT), Dalian, China, 2022, pp. 1-4, doi: 10.1109/ICEPT56209.2022.9873518.

[7] A. Hardock, Y. H. Kwark, R. Rimolo-Donadio, H. -D. Brüns and C. Schuster, "Using Via Stubs in Periodic Structures for Microwave Filter Design," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 4, no. 7, pp. 1212-1221, July 2014, doi: 10.1109/TCPMT.2014.2314074.

[8] A. Vardapetyan and C. -J. Ong, "Via Design Optimization for High-Speed Differential Interconnects on Circuit Boards," 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2020, pp. 1-3.

[9] J. Wang, C. Xu, S. Zhong, S. Bai, J. Lee and D. Kim, "Differential Via Designs for Crosstalk Reduction in High-Speed PCBs," 2020 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), 2020, pp. 145-149.

[10] J. Xu, L.Zhang, M.Sapozhnikov and J.Fan, "Application of Deep Learning for High-Speed Differential Via TDR Impedance Fast Prediction," IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity, 2018, pp.645-649.

[11] Janusz A. Dobrowolski, "Microwave Network Design Using the Scattering Matrix", Artech House, 2010.

[12] William R. Eisenstadt, "Microwave Differential Circuit Design Using Mixed Mode S-Parameters", Artech House, 2010.

[13] B. H. P. Naik, M. Misbahuddin and C. S. Paidimarry, "Analytical Delay Modeling of On-Chip Hybrid RGLC Interconnect," 2017 IEEE 7th International Advance Computing Conference (IACC), Hyderabad, India, 2017, pp. 505-509, doi: 10.1109/IACC.2017.0110.

[14] B. H. Naik, M. Misbahuddin and C. S. Paidimarry, "S-Parameter Modeling and Analysis of RGLC Interconnect for Signal Integrity," 2017 International Conference on Recent Trends in Electrical,

Electronics and Computing Technologies (ICRTEECT), Warangal, India, 2017, pp. 11-16, doi: 10.1109/ICRTEECT.2017.41.

[15] E. Bogatin, “Signal and Power Integrity Simplified”, 3rd Ed., Pearson Education, Inc., 2018.

[16] Douglas Brooks “Signal Integrity Issues and printed Circuit Board Design” Prentice Hall, June 2003.