Multi substrate voltage control for Current Starved Voltage Controlled Oscillator Design

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Abstract – Voltage control oscillator (VCO) is the major constituting unit in analog and digital circuit design. They have a significant role in different communication system designs. Among different forms of VCO design ring oscillators have most effectively been used. Several methods are used to create ring oscillators. Each inverter stage in a ring oscillator introduces a delay that affects oscillation frequency, the delay needs to be controlled. Managing the current available to charge or discharge at each stage is one method of controlling the delay which is referred to as current starved ring voltage-controlled oscillator (CSVCRO). The CSVCRO regulates the current supplied to each delay cell for charging and discharging rates of the capacitive load in the circuit which is achieved by modulating the turn-on resistance of pull-up and pull-down transistors via current mirror circuit. The control, however, limits its usage in a broader context and hence minimizes the tuning range and frequency stability. In this paper, a new bulk biasing approach for CSVCRO is proposed which controls the threshold voltage and improved the overall operational performance of a VCO design.

Keywords- Voltage Controlled Oscillator, current starved ring voltage-controlled oscillator, bulk biasing, frequency stability.

I. INTRODUCTION

One of the key components of both analog and digital circuits is a voltage-controlled oscillator (VCO). [1], [2], [3]. The primary component of phase locked loop (PLL) and clock generator circuits in contemporary microcircuits, for instance, is a VCO. Because of the impact of stray capacitance on the IC package's pins, clocks must not be fed into chips. On-chip oscillators are needed to produce clocks in high-speed circuits. Although LC oscillators [4] have gained popularity recently for their good phase noise performance, their tuning range is only about 10–20%, and on-chip spiral inductors take up a large amount of chip space. However, ring oscillators are more commonly used than LC oscillators because they typically have a wider tuning range and take up less on-chip integration space. Connecting an odd number of inverters and providing feedback from the last one's output to the first one's input are necessary for the design of a ring oscillator. In 0.18μm technology, the achieved frequencies are usually several hundred MHz to GHz, since the oscillation frequency is determined by the number of stages and the delay in each stage, which is very small for an inverter. It is sometimes unacceptable to have so many stages to achieve low frequency output. [5]. However, increasing driving capability has the disadvantage of using a lot of power. Ring oscillators are essential components used in the design of both digital and analog circuits. They are also widely utilized in a variety of electrical systems, such as clock generators, frequency dividers, and phase-locked loops. The ring oscillator circuit is made by connecting an odd number of inverting stages with a closed loop. Each step includes an inverter constructed with complementary metal-oxide-semiconductor (CMOS) technology [6-9]. The ring oscillator can produce a self-sustaining oscillation thanks to the delay that is added to each step.
The primary determinants of the oscillation frequency of the ring oscillator are the propagation delays of the different stages and the total delay imposed by the entire loop [10,11]. More stages can be added to increase the oscillation frequency, but fewer stages result in a lower frequency. The oscillation frequency can be further changed by adding more capacitive components or changing the transistor sizes. In digital systems, the ring oscillator is frequently used as a clock generator to produce timing signals for synchronous operation. To distinguish between higher and lower frequencies, it can also be utilized as a frequency divider. Furthermore, the ring oscillator is an essential component of phase-locked loops since it offers a reliable reference signal for frequency synthesis [12-17]. Careful consideration must be given to variables like transistor size, supply voltage, and load capacitance when constructing a ring oscillator.

The circuit's power consumption, frequency stability, and signal integrity are all directly impacted by these variables. Noise sources and process heterogeneity make it difficult to establish consistent performance. The final point is the ring oscillator, a flexible circuit with multiple applications in electrical systems. Its self-oscillating nature, simplicity, and scalability make it an essential component of many analog and digital systems. The current starved ring oscillator is an optimal design in this domain. This paper presents a current-starved ring VCO circuit that utilizes reverse voltages at three different stages. This approach effectively enhances both the frequency output and the tuning range, making it suitable for large signal applications. By optimizing the voltage conditions, we achieve improved performance characteristics that can be beneficial for various high-frequency applications. The paper's structure is outlined as: discussion on the standard ring oscillator, examination on CSVCRO, intended ring VCO and in-depth analysis with comparison of the simulation outputs and transient characteristics of the VCOs are provided. The contribution to the developed work is outlined as follows.

Contribution:

This paper presents the design of three distinct VCOs, emphasizing characteristics such as high frequency.

a) The initial VCO design is crafted employing a single-ended CMOS inverter ring oscillator, utilizing solely NMOS reverse biasing (NMOS CSVCRO). A broad tuning range, from 9.058 GHz to 174.9 MHz, is attainable through reverse bias technique. This range is achieved by modulating the NMOS substrate voltage, ranging from 100mV to 300mV, with a controlled voltage of 900mV to 400mV.
b) The second design VCO is constructed using PMOS substrate reverse biasing (PMOS CSVCRO) with a broad tuning range spanning from 8.063GHz to 129.7MHz is attainable through the reverse bias technique. This range is achieved by modulating the PMOS substrate voltage from 1.1 V to 1.3 V with controlled voltage 900mV to 400mV.
c) The third design constructed CMOS inverter ring oscillator using both NMOS and PMOS reverse biasing (Joint CSVCRO) with a broad tuning range from 8.467GHz to 273.9MHz.is attainable through the reverse bias technique. This range is achieved by modulating the NMOS substrate voltage from 100mV to 300mV and PMOS substrate voltage from 1.1 V to 1.3 V with a controlled voltage of 900mV to 400mV.

Circuit is implemented utilizing a 45nm with supply voltage of 1V. The outcomes demonstrate superior frequency performance and lower power consumption when compared with the existing current-starved ring VCO employing varying numbers of inverter stages. To present the outlined work, this paper is presented in 5 sections. Conventional design of voltage control oscillator is presented in section II. The proposed approach of VCO operation using multi substrates voltage control for current starved VCO is presented in section III. Simulation results and conclusion of the outlined work are presented in section VI and V respectively.

II. VOLTAGE CONTROLLED OSCILLATOR (VCO)

An amplifier that generates its own input signal is called an oscillator. An oscillator's main function is to create a given waveform at a fixed peak amplitude and frequency and to keep it within predetermined frequency and amplitude bounds. A Voltage Controlled Ring Oscillator (VCRO) is a type of oscillator that generates a resultant frequency based on an input control voltage. A chain of odd numbered single-ended inverters is used in the simplest CMOS ring oscillators. The first stage's input receives the output of the Nth stage. Due to the ring oscillator's odd number of inversions, there are no stable operation point exits. It consists of a series of inverters or amplifiers arranged in a ring configuration, typically odd number of inverters, in Figure 1 we have three inverters (I1, I2, and I3) configured in a feedback loop. The output of inverter I1 is linked to the input of I2, output of I2 feeds into I3, and the output of I3 loops back to the input of I1, creating a closed circuit. Each inverter refers to a delay cell that delays the signal before passing it to the next stage in the ring. The amount of delay introduced by each unit contributes to the overall oscillation period of the VCO.

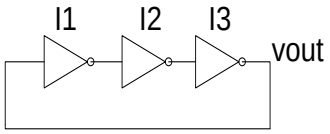

Figure 1. CMOS ring oscillator

Ring structures, relaxation circuits, or an LC resonant circuit can all be used to construct a CMOS VCO. Due to the high-quality factor Q that resonant networks can achieve, the LC design offers the best noise and frequency performance. Nevertheless, incorporating premium inductors into a CMOS process flow raises the chip's cost and complexity and adds issues like eddy current control. In contrast, ring oscillators may require less die area than LC

designs and can be constructed using any common CMOS process. Ring architecture can be used to provide wide tuning ranges and multiple output phases, and the design is simple. We offer a design in this brief that enhances CMOS ring oscillators' general properties to match those of LC designs. As illustrated in Figure2, each inverter is constructed using CMOS technology, incorporating PMOS (M1, M2, and M3) transistors and NMOS (M4, M5, and M6) transistors. This configuration allows for efficient switching and low power consumption while maintaining high performance. The use of PMOS and NMOS transistors in this arrangement ensures that the inverters can operate effectively across a wide range of voltages, contributing to the enhanced frequency and tuning range of the VCO circuit.

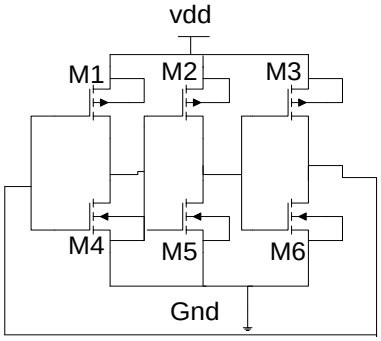

Figure 2. CMOS ring oscillator with 3 stage delay cells

An oscillator functions as an inverter or amplifier that produces output without requiring any input. The expected result is a predefined waveform through steady high amplitude and a specified frequency. To achieve these sustained oscillations, it should satisfy Barkhausen criteria, which state.

1. Each oscillation must impart a 180-degree phase shift.
2. It must maintain unity gain.

Here each delay cell of a ring oscillator must contribute a phase shift of $\frac{\pi}{N}$ where N denotes the overall amount of delay elements. The continuing π phase shift in a ring oscillator is a crucial mechanism for achieving sustained oscillations. This phase shift is accomplished through DC phase inversion, which necessitates an odd number of delay elements in the oscillator's loop. Equation 1 states the total time of the signal (T) which transmits through each time delay (t_d)of the delay cell to complete one cycle is called period of ring oscillator.

$$T = t_d \times 2 \times N \tag{1}$$

Where N= amount of delay cells ,2 represents the transitions of the signals from 0V to 1V and 1V to 0V. From equation (1) the frequency is expressed as,

$$F = \frac{1}{T} \tag{2}$$

From equation (1) & (2) the frequency of oscillations is expressed as,

$$F = \frac{1}{2 \times N \times t_d} \tag{3}$$

The frequency of a voltage-controlled ring oscillator is determined by the number of delay cells (N) and the time delay of each cell (t_d), since the frequency of oscillations is inversely proportional to the time delay of each cell. The conventional ring oscillator-based VCO controls the oscillation frequency by means of variable bias currents. However, when the bias current is relatively low, the VCO's voltage swing will slow down (have a longer rise/fall time). That is undesirable in certain applications. Additionally, as the bias current rises, the current source PMOS transistors voltage headroom will decrease. As previously mentioned, if the oscillations frequency is to be changed, we should consider two criteria from equation (2): either the delay time of the respective delay cell needs to be changed, or the number of delay stages should be increased or decreased based on the application. The only way to change the area of the chip in this case is to change the delay of the corresponding delay cell (t_d), as the number of delay stages cannot be changed. Controlling the voltage, which is accomplished by controlling the current supplied to each delay cell, allows one to reduce the delay of the corresponding delay stage. This also controls the charging and discharging rates of the circuit's capacitive load. A CSVCRO can be used to achieve this. Via a current mirror circuit, controlled voltage (V_{ctrl}) modulates the pull-up and pull-down transistors' turn-on resistance, controlling the output

frequency. The frequency of oscillations increases when the control voltage (V_{ctrl}) is high because more current flows, which lowers resistance and delays for each cell. On the other hand, less current flows when the control voltage (V_{ctrl}) is low, which raises resistance, increases delay for each cell, and lowers oscillation frequency. Nevertheless, the current modulated turn-on resistance-controlled voltage design has a narrow control range, which leads to reduced frequency stability. For various CMOS designs, a bulk bias is used to stabilize the braider range of frequencies.

III. BULK BIAS CONTROL FOR CURRENT STARVED VCO OPERATION

The voltage-controlled oscillator (VCO) is essential to communication systems due to its low power consumption, wide frequency range of operation, and high integration capability. This electronic device uses a resonant circuit, feedback, and amplification to produce a repeating voltage waveform at a particular frequency. The frequency or rate of repetition per unit of time changes in response to an applied voltage. VCOs are an essential part of almost every analog and digital system, such as frequency synthesizers, clock recovery circuits, and phase locked loops. For a VCO to be used, it must have a high frequency, low power consumption, phase stability, a large electrical tuning range, frequency linearity on the control voltage, small size, low cost, and a high gain factor. The design of the ring VCO includes tradeoffs between area, speed, power, frequency, and different application domains. The current starved ring VCO is shown in Figure 3. The output frequency can be adjusted by varying the delay of each inverter stage.

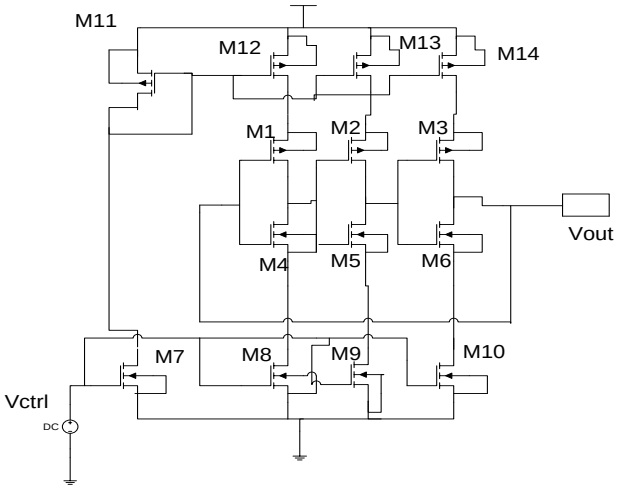

Figure 3. Current starved voltage-controlled ring oscillator (CSVCRO)

While M13, M14, M9, and M10 act as the current source and sink, M1, M2, M3, M5, M6, and M7 form a back-to-back inverter chain. As a current-limiting circuit, the current mirror circuit regulates the amount of current flowing through M11 and M12, which in turn controls the oscillation frequency. Although the CSVCRO can be designed in a variety of ways, it has excellent frequency performance given the limitations of 180nm technology. By applying reverse bulk voltage in three different configurations—NMOS reverse bulk CSVCRO, PMOS reverse bulk CSVCRO, and a joint bulk bias current-starved circuit—this circuit presents a novel way to improve the act of a current-starved ring VCO. By applying a negative voltage to the transistors' bulk terminal, this method can alter the transistors' threshold voltage and, in turn, the VCO's overall performance. We can increase the tuning range and frequency stability by adjusting the bulk bias.

Threshold voltage (V_{th}) of a MOSFET is adjusted by altering the substrate voltage applied to both NMOS and PMOS transistors. Equation (4) governs the threshold voltage (V_{th}) of the circuit, which in turn is influenced by the reverse bulk voltage, thereby regulating the frequency of oscillations

$$V_{th} = V_{t0} + \gamma \left(\sqrt{2\emptyset_f + V_{sb}} - \sqrt{2\emptyset_f}\right) \quad (4)$$

Where $\gamma = \frac{\sqrt{2qN_A\varepsilon_{si}}}{C_{ox}}$

V_{sb}= substrate bias voltage, V_{th} = threshold voltage, N_A = Acceptor impurity, ε_{si} =Permittivity of silicon, $\emptyset_f$ = fermi potential, V_{t0}=threshold voltage for V_{sb} =0V. So, Increasing the negative bulk voltage (V_b)will lead to an increase in the threshold voltage (V_{th}),as a result the delay of the circuit increases which results in decrease in frequency of oscillations from the equation(4) and conversely, increasing the positive bulk voltage will result in a decrease in the threshold voltage (V_{th}),as a result the delay of the circuit deceases which results in the increase in the frequency of oscillations.

The substrate terminal is linked to the reverse substrate bias voltage (V_{cn}) for NMOS and (V_{cp}) for PMOS, while the supply voltage is 1v. These proposed circuits are presented where the output frequency of oscillations is based on the reverse bulk voltage.

In the Current Starved Voltage Controlled Ring Oscillator (CSVCRO) shown in Figure 4, the control voltage (V_{ctrl}), which varies from 400 mV to 900 mV, plays a crucial role in determining the oscillation frequency. This voltage controls the M7 transistor, which acts as a current-limiting device for the delay elements in the ring oscillator. The circuit operates with a 1V supply voltage. As (V_{ctrl}), increases, the M7 transistor allows more current to flow, resulting in faster charging and discharging of the internal capacitances in the inverter stages. This reduces the propagation delay and consequently increases the oscillation frequency. On the other hand, when (V_{ctrl}), decreases, the current flow is restricted, leading to slower transitions, increased delay, and a lower oscillation frequency. Thus, the frequency of the CSVCRO is directly dependent on the control voltage, enabling dynamic and precise frequency tuning based on voltage variation. In the proposed three-stage current-starved ring oscillator, the PMOS substrates are connected to their drains, and the NMOS substrates are biased with a voltage (V_{cn}), ranging from 100 mV to 300 mV. This substrate biasing reduces the threshold voltage (V_{th}),of both PMOS and NMOS transistors due to the body effect. A lower (V_{th}),increases the transistors' drive strength, allowing faster switching and reduced delays in each stage. As a result, the overall frequency of oscillation Transistors M1, M3, M4, M5, and M6 operate as back-to-back CMOS inverters that provide feedback. While M11 and M12 act as the current mirror circuit to control current flow, M9, M10, M13, and M14 act as current sources and sinks.

The layout area of the NMOS reverse-biased CSVCRO is 14.4493 μm², as shown in Figure 5. It includes the inverter stages, current-starving NMOS transistors, and routing for the reverse substrate bias voltage (V_{cn}).The compact layout reflects efficient design suitable for high-frequency, low-power applications

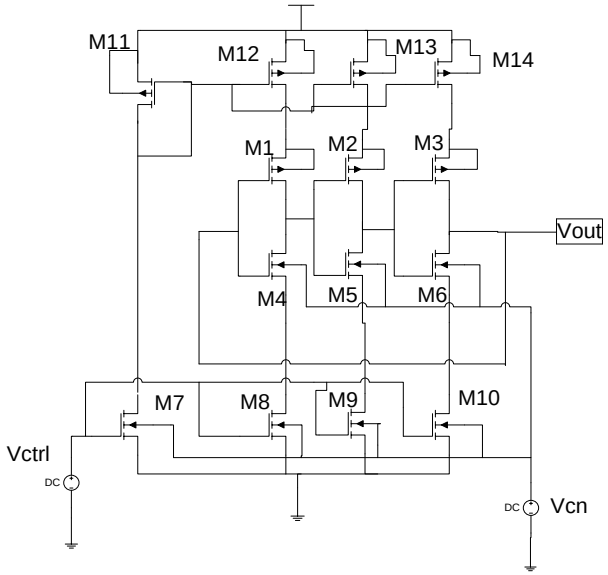

Figure 4. CSVCRO with NMOS reverse substrate voltage (V_{cn})

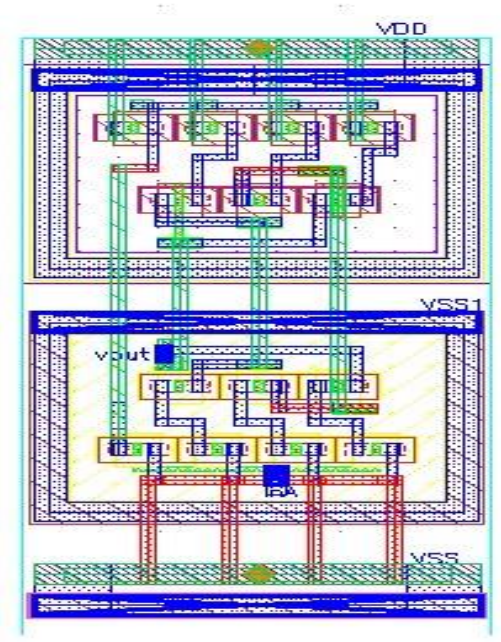

Figure 5. Layout of CSVCRO with NMOS reverse substrate voltage (V_{cn})

There is a three-stage delay CSVCRO in the second suggested design. In this design, all NMOS transistors have their substrate terminals tied to their sources, resulting in no body effect and maintaining their nominal threshold voltage. The PMOS transistors, however, have their substrate terminals connected to a higher substrate voltage (V_{cp}), ranging

from 1.1 V to 1.3 V, while their sources are typically at 1 V. This introduces a forward body bias in the PMOS devices, reducing their threshold voltage. As a result, the PMOS transistors switch faster, decreasing the delay per stage and thereby increasing the overall oscillation frequency of the ring oscillator. Transistors M1, M3, M4, M5, and M6 operate as back-to-back CMOS inverters that provide feedback. While M11 and M12 act as the current mirror circuit to control current flow, M9, M10, M13, and M14 act as current sources and sinks. Additionally, the voltage (V_{ctrl}), which ranges from 900mV to 400mV, is controlled by the M7 transistor. Figure 6 illustrates this with a supply voltage of 1V. The layout area of the PMOS reverse-biased CSVCRO is 15.2222 μm², as shown in Figure 7, encompassing all inverter stages, current-starving PMOS transistors, and necessary routing for the substrate bias voltage.

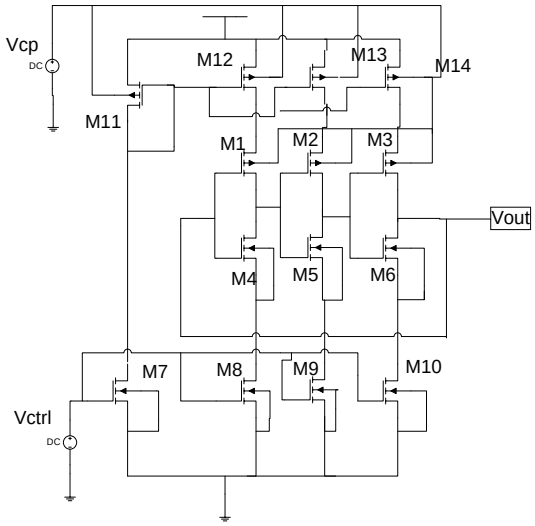

Figure 6. CSVCRO with PMOS reverse substrate bias voltage(V_{cp})

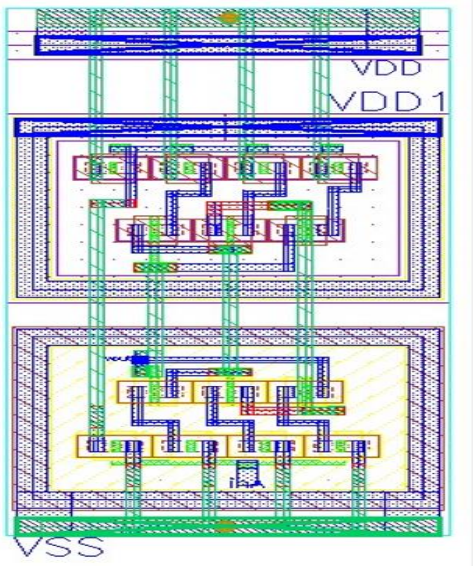

Figure 7. CSVCRO with PMOS reverse substrate bias voltage(V_{cp})

In this design, the substrate terminals of NMOS transistors are connected to a controlled voltage (V_{cn}) between 100 mV and 300 mV, while PMOS substrates are connected to a controlled voltage (V_{cp}), from 1.1 V to 1.3 V. Because NMOS sources are typically at 0 V, and PMOS sources near 1 V, both substrate voltages are higher than their respective source voltages. This creates a negative source-to-substrate voltage (V_{sb}) for both transistor types, causing forward body biasing. Forward body bias reduces the threshold voltages of NMOS and PMOS transistors, enhancing their drive strength and switching speed. As a result, the delay in the circuit decreases and the overall oscillator frequency increases. In Figure 8 there is a third proposed design, which incorporates three delay stages of a current-starved ring oscillator. Transistors M1, M2, M3, M4, M5, and M6 operate as back-to-back CMOS inverters that provide feedback. While M11 and M12 act as the current mirror circuit to control current flow, M9, M10, M13, and M14 act as current sources and sinks. Furthermore, with a supply voltage of 1V, the M7 transistor regulates the voltage (V_{ctrl}), which ranges from 900mV to 400mV. The layout area of the joint NMOS and PMOS reverse-biased CSVCRO is 16.8073 μm², as shown in Figure 9, including inverter stages, both NMOS and PMOS current-starving transistors, and substrate bias routing. The layout area results reflect a trade-off between design complexity and performance. The NMOS-only design is most area-efficient, while the joint configuration, offering potentially better frequency control and performance balance, requires more silicon real estate. The PMOS design sits between the two in terms of area and performance characteristics.

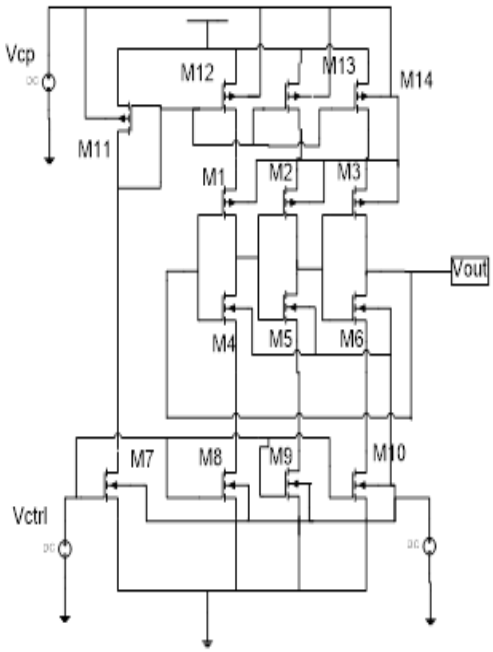

Figure 8. CSVCRO with joint transistors reverse substrate bias voltage

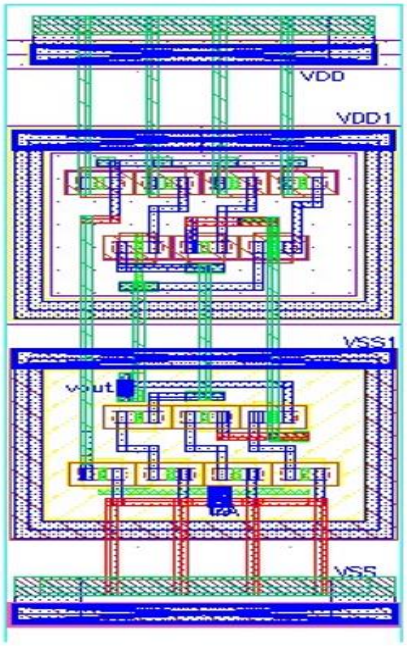

Figure 9. Layout of CSVCRO with joint transistors reverse substrate bias voltage

The frequency range and linearity of the VCO are determined by the variation of the control voltage (V_{ctrl}). The control voltage is used to adjust the frequency output. Each stage's μ delay is represented by equation (5) as follows:

$$\mu = \frac{V_{osc}C_p}{I_{cntr}} \tag{5}$$

where I_{cntr} is the control current, V_{osc} is the oscillation amplitude, and C_p is the parasitic capacitance of nMOS and pMOS transistors. The current-starved VCO's oscillation frequency in terms of control current is given by equation (6):

$$Freq_{osc} = \frac{I_{cntr}}{2NV_{osc}C_p} \tag{6}$$

The benefit of this setup is that by altering the control voltage, the oscillation frequency can be adjusted over a large range.

IV. SIMULATION RESULT

Cadence software is used to model the proposed current-starved VCRO under constant supply voltage conditions in 45-nm Gpdk CMOS technology. Three distinct circuits have their reverse body voltage adjusted, which results in varying frequency oscillations. Changing reverse bias voltage, varying controlled voltage, and constant supply voltage levels all modulate the output frequency. The first design's output results, shown in Figure 10, show how changing the NMOS substrate voltage from 100mV to 300mV impacts the output frequency. This indicates that as the controlled voltage (V_{ctrl}) rises from 400V to 900mV and vice versa, the output frequency rises as well. Important trends in frequency behavior are revealed by the NMOS Reverse Bias Voltage Controlled Oscillator analysis and the frequency spans from 8.5GHz to 9.058GHz at 900mV controlled voltage (V_{ctrl}). The frequency typically falls as the substrate voltage becomes less negative (from 100mV to 300mV), The controlled voltage has a stronger effect on frequency even though the substrate and controlled voltages are independent. These results show that under extremely positive substrate voltages and lower controlled voltages, the oscillator performs better (at higher frequencies).

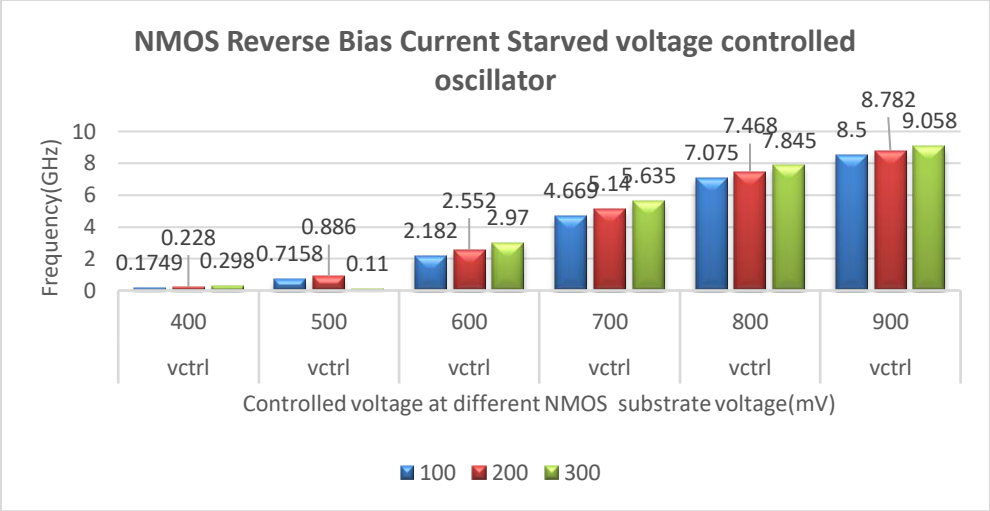

Figure 10. Output frequency at NMOS body bias at variable supply voltages

The output waveform of a three-stage CSVCRO is shown in Figure 11, which shows the NMOS reverse bias voltage with the supply voltage at 1V and the controlled voltage at 400mV. A transient voltage response with consistent oscillatory behavior over time is represented by the waveform that is provided. With a peak-to-peak amplitude of 1000 mV, the voltage fluctuates periodically between a minimum of -50 mV and a maximum of 950 mV. A symmetric oscillation is evident around the midpoint of the waveform, which is centered around an average voltage of 450 mV. Systems functioning in a steady state following an initial transient exhibit this behavior. Based on the 0.5 nanosecond interval between consecutive peaks, the waveform's frequency is estimated to be around 2 GHz. This high-frequency oscillation implies that the system is a component of an electronic circuit that operates quickly, like an RF oscillator or a clock signal. The system's stability during steady-state operation is demonstrated by its constant amplitude and steady periodicity.

There is a noticeable transient response at the waveform's beginning (t = 0ns). This suggests that the system was first excited or disturbed before quickly, in about 0.2 nanoseconds, settling into its steady oscillatory state. The system's rapid stabilization indicates that it is built for high-speed operation with little delay in reaching its operational state. All things considered, the waveform shows a stable, high-frequency oscillatory system with distinct features.

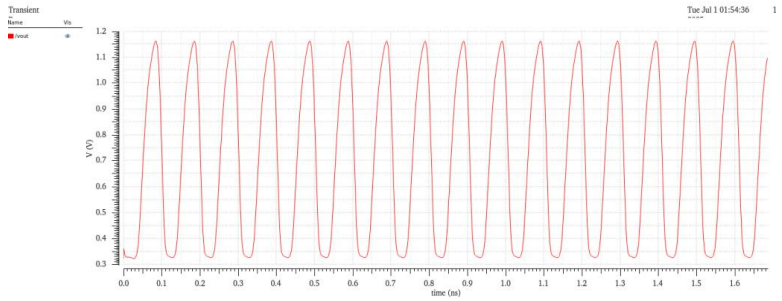

Figure 11. Simulation results with reverse bias with NMOS voltage-controlled ring oscillator

The frequency ranges of the second suggested design are shown in Figure 12, where the PMOS substrate voltage varies between 1.1V and 1.3V, resulting in frequency variations between 8.063GHz and 7.733GHz at control voltage (V_{ctrl}) between 900mV.

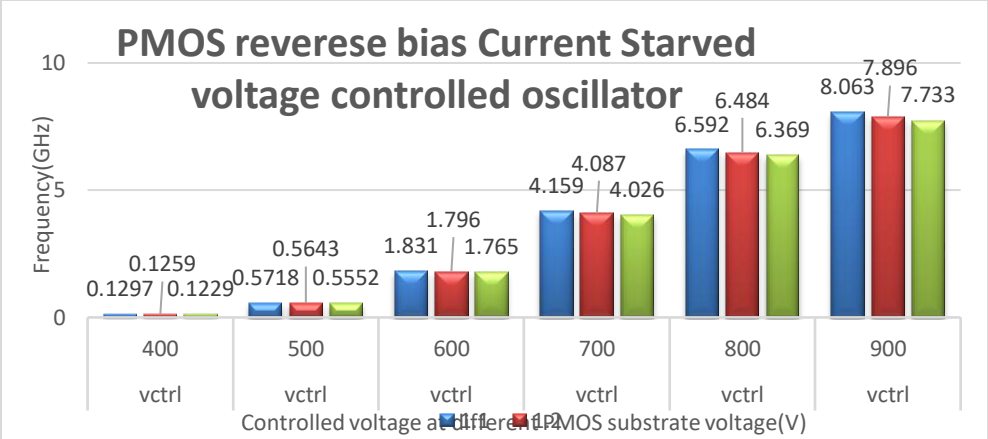

Figure 12. Output frequency at PMOS body bias at different supply voltages.

The output waveform of a three-stage CSVRO is shown in Figure 13, which shows the PMOS reverse bias voltage with the supply voltage at 1V and the controlled voltage at 400mV. The transient response of a voltage signal measured in milli-volts (mV) over time in milliseconds (ms) is depicted in the provided graph. The first 0.2 ms show a brief transient phase during which the voltage varies slightly before stabilizing into an oscillatory pattern. A full swing of 900 mV per cycle is indicated by the peak voltage reaching about 900 mV and the minimum voltage staying near 0 mV. Following the initial transient, the waveform stabilizes into a periodic sinusoidal pattern, indicating that the circuit rapidly achieves steady-state behavior.

By measuring the distance between successive peaks, we can calculate the time by looking at the oscillation frequency. Based on the graph, a frequency of 2 kHz (f = 1/T) corresponds to a time interval of roughly 0.5 ms between two adjacent peaks. The circuit has little damp and sustains a steady oscillation, as evidenced by the waveform's constant amplitude and frequency. Circuits with reactive components, like capacitors and inductors, which periodically store and exchange energy, often exhibit this type of response.

The initial transient response indicates that the system was either excited by an initial impulse or by a sudden input voltage. Rapid waveform stabilization within 0.2 ms suggests that the circuit has a high-quality factor (Q), which translates to low cycle energy loss. This signal may indicate a feedback-driven amplifier, a resonant RLC circuit, or an LC oscillator given its peak voltage of 900 mV and frequency of 2 kHz. When stable frequency generation is needed in signal processing applications, waveform generators, and communication systems, such oscillatory behaviors are essential.

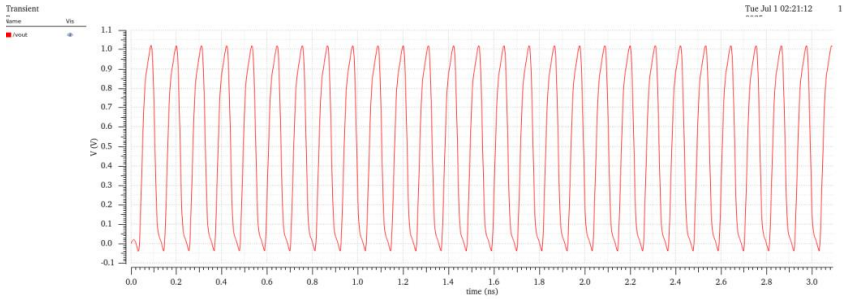

Figure 13. Simulation results with reverse bias with PMOS VCRO

The third suggested design's results show that when the PMOS substrate voltages are adjusted from 1.1V to 1.3V and NMOS substrate voltages are adjusted from 100mV to 300 mV, at a controlled voltage (V_{ctrl}) of 900mV the frequency varies from 7.841 GHz to 8.467 GHz.An NMOS & PMOS substrate bias voltage-controlled oscillator's frequency response at various controlled voltages and substrate bias conditions is shown in Figure 14. The data indicates that the oscillation frequency likewise decreases as the controlled voltage drops from 900 mV to 400 mV. The maximum frequency at 900 mV is recorded at 7.841 GHz for V_{cn}=100 mV bias, V_{cp} =1.1V,8.403 GHz for V_{cn}=200 mV bias, V_{cp}

=1.2 V, and 8.467 GHz for V_{cn}=300 mV bias, V_{cp} =1.3 V. The associated frequencies decrease to 4.585 GHz, 4.957GHz, and 5.33GHz for respective V_{cn} &V_{cp} when the controlled voltage is lowered to 700 mV.
At lower controlled voltages, this trend continues, with the frequency decreasing even more. The frequency values for for respective V_{cn} &V_{cp} bias voltages at 500 mV are 0.7037 GHz, 0.8548 GHz, and 1.04 GHz, respectively. Lastly, the oscillator functions at the lowest frequencies shown in the chart at 400 mV: 0.1689 GHz, 0.2142 GHz, and 0.2739 GHz for bias voltages of for respective V_{cn} &V_{cp}. Higher substrate bias voltages result in higher oscillation frequencies, which is an important consideration when designing tunable oscillators for high-frequency applications, according to the data, which clearly shows a direct relationship between the controlled voltage and oscillation frequency.

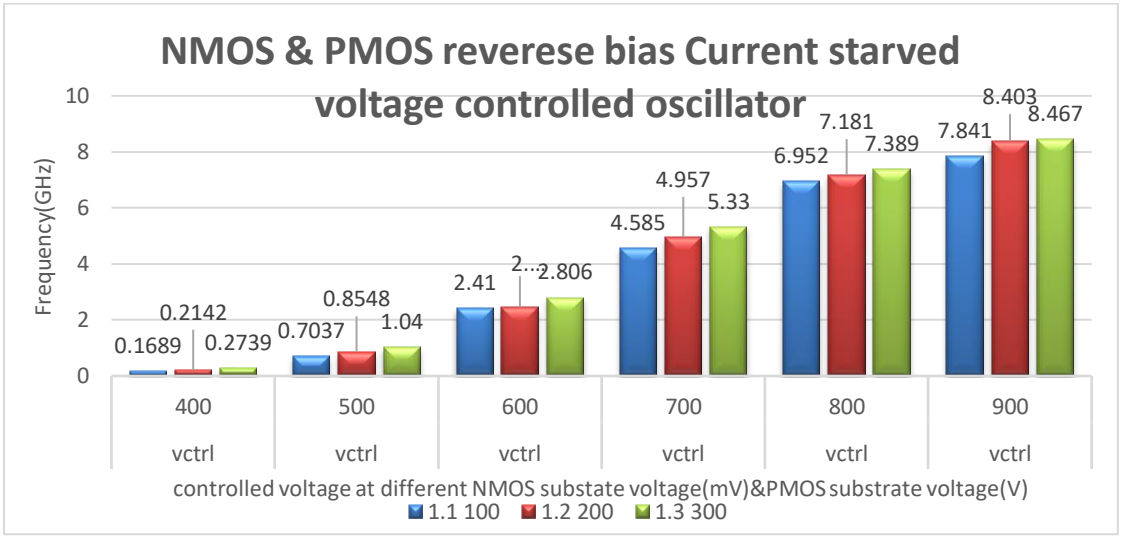

Figure 14. Output frequency at Joint CSVCRO body bias at different supply voltages.

Figure 15 shows the simulated output of both Joint CSVCRO, which provides less frequency of oscillations when compared to the above type of oscillator.

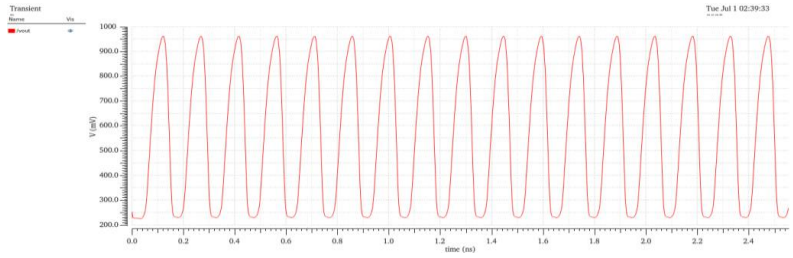

Figure 15. Simulation results with reverse bias with NMOS & PMOS VCRO

Figure 16 shows the maximum frequency 9.058GHz obtained by the NMOS CSVCRO. The low oscillation frequency of 8.063 GHz has been achieved by the PMOS CSVCRO. The joint CSVCRO has achieved moderate oscillation frequency, which is 8.469 GHz. at 900mV controlled frequency and if its NMOS reverse, biasing its V_{cn} ranges from 100mV to 300mV and for PMOS biasing its V_{cp} ranges from 1.1V to 1.3V

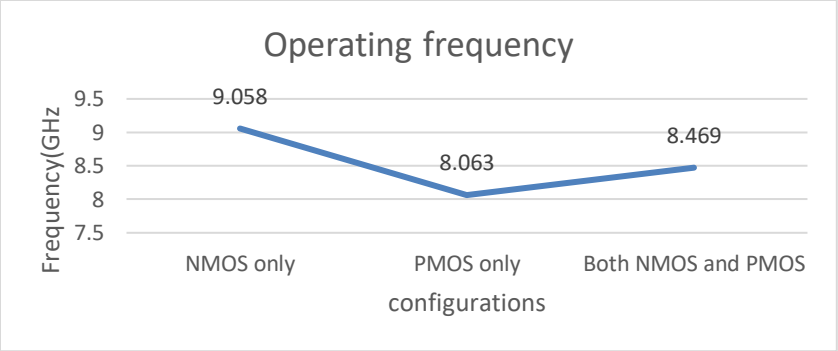

Figure 16. Frequency response with three different designed oscillators

Additionally, this graph shows the frequency response of three distinct voltage-controlled ring oscillators (VCROs) with 900mV controlled voltage (V_{ctrl}) and substrate biases at 100mv for NMOS CSVCRO,1.1 V for PMOS CSVCRO and for joint CSVCRO it has 100mV for NMOS substrate voltage and 1.1V for PMOS substrate voltage, that operate at a 1V supply voltage.

Based on supply voltage, operating frequency, Table 1 compares several voltage-controlled oscillators (VCOs) from different reference papers. Although the suggested circuit uses more power, it performs noticeably better in terms of frequency than earlier designs. In contrast to the 1.1218 GHz frequency reported by Kumar et al. (2012) for NMOS biasing, the suggested NMOS-biased oscillator operates at 9.058 GHz, Kumar et al.'s PMOS-biased design achieved 1.009 GHz, whereas the suggested PMOS-biased circuit achieves 8.063 GHz. The suggested design's joint biasing approach yields 8.469 GHz while Kumar et al.'s study found 0.81873 GHz.

Other cited studies, including Das et al. (2020) and Panigrahi et al. (2010), described oscillators that operated between 1.22 and 3.22 GHz and 2.58 GHz, respectively. When compared to the suggested circuit, these designs show noticeably higher power consumption. Low-frequency designs with unknown power consumption were presented by Almeida et al. (2020) and Suman et al. (2016). They operated at 84.81 kHz and 0.1703 GHz, respectively. According to the comparison, the suggested circuit is better suited for high-performance applications because it achieves much higher operating frequencies—especially when PMOS biasing.

Table 1. *Comparison of VCO performance metrics*

Reference Paper		**Supply Voltage(V)**	**Operating Frequency**
[1]		1-3.2	84.81KHz
[2]		1.15	2.58GHz
[7]		1.5	1.22-3.22GHz
[12]	NMOS Biasing	1.8-1	1.1218 GHz
	PMOS Biasing	1.8-1	1.009 GHz
	Joint Biasing	1.8-1	0.81873 GHz
Proposed circuit with NMOS biasing		1	9.058 GHz
Proposed circuit with PMOS biasing		1	8.063GHz
Proposed circuit with joint biasing		1	8.469 GHz

V. CONCLUSION

In this work, three VCO designs based on CSVCRO architecture were analyzed and compared in terms of frequency performance and layout efficiency. Among the three, the NMOS reverse-biased design demonstrated the highest frequency range (9.058 GHz to 8.5 GHz) and the smallest layout area (14.4493 μm²), making it the most efficient for high-speed and low-area applications. The PMOS-biased design, while offering a lower frequency range, is useful where layout constraints are less critical. The joint NMOS & PMOS reverse-biased VCO provided a balanced performance with moderate frequency tuning and the largest area due to increased design complexity. Overall, reverse

body biasing proves to be an effective technique for frequency control and power optimization in VCO design, with NMOS-based configurations offering superior results in both frequency and silicon areas.

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