# DESIGN OF HAMMING CODE ENCODING AND DECODING BASED ON CLOCK GATING TECHNIQUE

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***Abstract***

The Hamming code encoder and decoder circuit is implemented using Clock Gating gate logic. Hamming code is one of the commonest codes used in the protection of information from error. It takes a block of k input bits and produce n bits of codeword. This work presents a way of designing (7, 4) Hamming encoder and decoder using Verilog HDL. The encoder takes 4 bits input data and produces a 7 bit codeword. The encoder was designed through the usual generator matrix multiplication while in the decoder design the computation of the syndrome vector was ignored. Meanwhile, the different states that can represent a particular input were calculated and the decoder was designed to identify each codeword representing a particular input. Clock gating is a technique which is used here for power reduction, in which the clock is disconnected from a device it drives when the data going into the device is not changing. This technique is used to minimize power. Results have shown that the method is also reliable. The proposed design, which is implemented in a FPGA Spartan Boart and Simulated and Synthesized by Modelsim and Xilinx for customized for the Communication.

***Keywords - Parity Bit, Clock Gating, Encoding, Decoding, Code word, VLSI design.***

## I. INTRODUCTION

In digital electronic projects, the encoder and decoder play an important role. It is used to convert the data from one form to another form. Generally, these are frequently used in the communication systems like telecommunication, networking, and transfer the data from one end to the other end. In the same way, it is also used in the digital domain for easy b transmission of data, placed with the codes, and then transmitted. At the end of the receiver, the coded data are collected from the code and then processed to display. This article discusses what are encoder and encoder, working and their applications.

### What are Encoder and Decoder?

The encoder is a device or a transducer or a circuit. The encoder will convert the information from one format to another format i.e like electrical signals to counters or a PLC. The feedback signal of the encoder will determine the position, count, speed, and direction. The control devices are used to send the command to a particular function. Hamming Codes are linear block codes designed to detect and correct errors introduced in message bits transmitted from an end to another through a communication channel. These are single error-correcting codes that offer ease in encoding and decoding. Hamming Code falls under the category of error correction coding and is a type of cyclic code.

In the year 1950, R W Hamming proposed an efficient array of algorithms as a technique for error correction, which was named hamming codes. The aim behind introducing it was to detect up to 2-bit errors at the same time and can correct a single bit error. We all are aware of the fact that message signal (in the form of bits) is transmitted from one end to the other via the proper channel in digital communication. However, during transmission, a high possibility of introduction of errors within the message bits exists because of factors like noise or any other interference. Thus, detection, as well as correction of errors at the receiver, is quite an important task and this can be achieved by introducing redundancies in the actual message bits. Error-correcting codes are used to deal with the introduction of errors while transmission. This includes error detection as well as correction.

Basically, error detection coding corresponds to the analysis where the receiver gets to know that error exists in the received sequence but fails to get the erroneous bit. While error correction coding corresponds to determining the actual bits, which is erroneous, and applying methods to correct the error bit.

Hamming codes are the ones that perform both error detection as well as error correction thereby giving rise to an efficient error correction coding system. Basically, in such error-correcting codes, redundancies are used for error detection and correction. This works in a way that, parity bits along with actual message bits are transmitted over the channel in a coded format. When the receiver gets the coded signal then it separates the parity bits from the message bit and simultaneously if the error is introduced then it gets also detected and further corrected.

## II. HAMMING CODE DESIGN

### HAMMING CODE Generation

Hamming code is a set of error-correction codes that can be used to **detect and correct the errors** that can occur when the data is moved or stored from the sender to the receiver. It is **technique developed by R.W. Hamming for error correction**.

Redundant bits are extra binary bits that are generated and added to the information-carrying bits of data transfer to ensure that no bits were lost during the data transfer.
The number of redundant bits can be calculated using the following formula:

$$2^r \geq m + r + 1$$

**where, r = redundant bit, m = data bit**

### HAMMING PARITY GENERATION

**Hamming Parity bits –**

A parity bit is a bit appended to a data of binary bits to ensure that the total number of 1’s in the data is even or
odd. Parity bits are used for error detection. There are two types of parity bits:

**1.Even parity bit:**In the case of even parity, for a given set of bits, the number of 1’s are counted. If that count is odd, the parity bit value is set to 1,making the total count of occurrences of 1’s an even number. If the total number of 1’s in a given set of bits is already even, the parity bit’s value is 0.

**2. Odd Parity bit –**

In the case of odd parity, for a given set of bits, the number of 1's are counted. If that count is even, the parity bit value is set to 1, making the total count of occurrences of 1's an odd number. If the total number of 1's in a given set of bits is already odd, the parity bit's value is 0.

**Example**

M = 1011 = 4

2^r ≥ m + r + 1

R=0

4>=4+2+1

2^3

8>=4+3+1=8

R=3

$2^0$,$2^1$,$2^2$ ---------- 1,2,4

**Encoding scheme**

S=m+r = 7

| 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|
| **D4** | **D3** | **D2** | **P4** | **D1** | **P2** | **P1** |
| **1** | **0** | **1** | **P3** | **1** | **P2** | **P1** |

| P4 | P2 | P1 | |
|---|---|---|---|
| **0** | **0** | **0** | |
| **0** | **0** | **1** | **1** |
| **0** | **1** | **0** | **2** |
| **0** | **1** | **1** | **3** |
| **1** | **0** | **0** | **4** |
| **1** | **0** | **1** | **5** |
| **1** | **1** | **0** | **6** |
| **1** | **1** | **1** | **7** |

P1 = P1,3,5,7 = P1,1,1,1 = 1

P2= P2,3,6,7 = P21,0,1 = 0

P4=P4,5,6,7= P4,1,0,1 = 0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|
| D4 | D3 | D2 | P4 | D1 | P2 | P1 |
| 1 | 0 | 1 | P4 | 1 | P2 | P1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |

**Decoding scheme**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|
| | D4 | D3 | D2 | P4 | D1 | P2 | P1 |
| | 1 | 0 | 1 | P4 | 1 | P2 | P1 |
| Encoded | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| Error add | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

P1,P2,P4

P1 = 1,3,5,7 = 1 1 1 1 = 0

P2= 2,3,6,7 = 0 1 1 1 = 1

P4=4,5,6,7= 0 1 1 1 = 1

P4 P2 P1 = > 110 = 6

1011

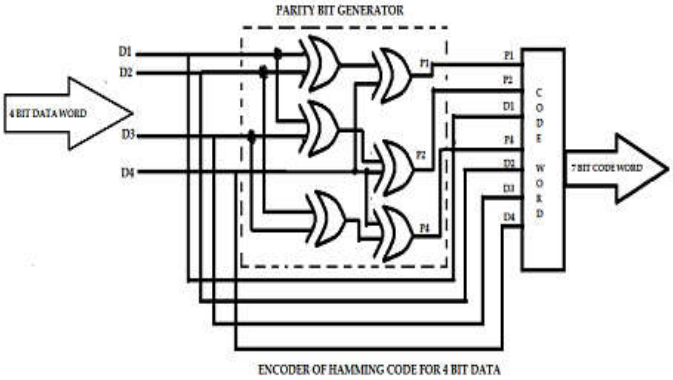
## III. PROPOSED SYSTEM

These pipeline computer systems, each stage consists of register and logical elements that implement a selected function. These systems are scaled by varying the number of pipeline stages. Values of the FPGA inputs can be used as initial values. The regular structure is another advantage of pipeline computer systems. It simplifies the placing stage of FPGA development. As basic test functions, generator error-detecting codes are proposed. The input data for these generators is the input data of the test system. Output data consists of error detection bits calculated for this input data. The result of pipeline's each stage operation is the intermediate value of error detection bits. Proposed circuits of hamming code are designed for 4 bit data word. Thus we require 3 parity bits to form 7 bit code word. There has an encoder and a decoder in the proposed circuit to encode and decode the data for error detection and correction. This Complete Error Correction Code design will implemented as Pipelined and clock Gating Technique.

### ENCODER CIRCUIT

Data word is applied as an input in the encoder circuit which performs XOR operations on the given data word and thus the required parity bits are generated from the parity generator. Parity bits and data bits together form the code word. An encoder circuit of hamming code for 4 bit data word is shown below.

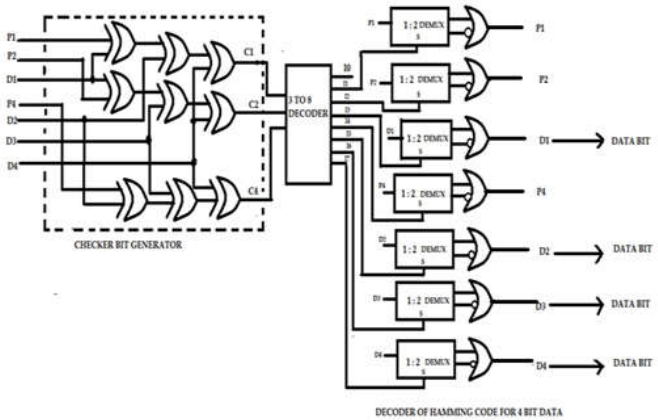
Following this circuit pattern we can design an encoder circuit of hamming code for 8bit data word and realized.




ENCODER OF HAMMING CODE FOR 4 BIT DATA

## DECODER

In the decoder circuit, code word is applied as input. Then check bits are generated by the checker bit generator to check the parity bits. These check bits locate the error in the code word by means of decoder circuit. The Output of decoder enables a demultiplexer which is connected to the input code words. If no error occurs then the select line of demultiplexer flows the input form line I0 and the I1 is set to logic '1'. So from the logic OR gate we can obtain the data. Now if an error occurs then the select line of the demultiplexer flows the code word from line I1 and I0 is set to logic '0'. Thus inverting the bits, the error bit is corrected and thus we can obtain the error free data. A decoder circuit of hamming code for 4 bit data word is also shown below.




DECODER OF HAMMING CODE FOR 4 BIT DATA

## PROPOSED SYSTEM TECHNIQUE:

- Clock Gating Technique based Pipelined ECC

**ADVANTAGES:**

- Less Delay compared all Existing Designs
- Good Power Performance

**APPLICATIONS:**

- Communications and signal processing systems
- Mobile Communication Application

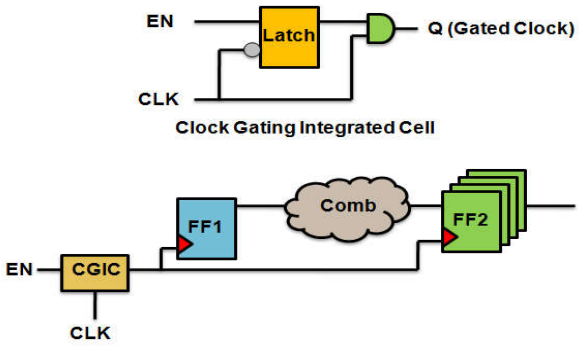
## IV. CLOCK GATING:

Clock gating is a well-known technique to reduce chip dynamic power. Recent clock gating techniques based on ACG(Adaptive Clock Gating) and instruction level clock gating. clock gating technique reduces not only switching activity of functional blocks in IDLE state but also dynamic power in running state. Our modified ACG (Adaptive Clock Gating) can automatically enable or disable the clock of the functional block. Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree.

Everywhere acceptance of portable devices such as cell phones, PDAs and mp3 players has much research in the development of technique for low-power design. The continuous decrease in the minimum feature size of transistors which increase of both device density and design complexity. The overall power dissipation on a chip is due to clock and data-path.

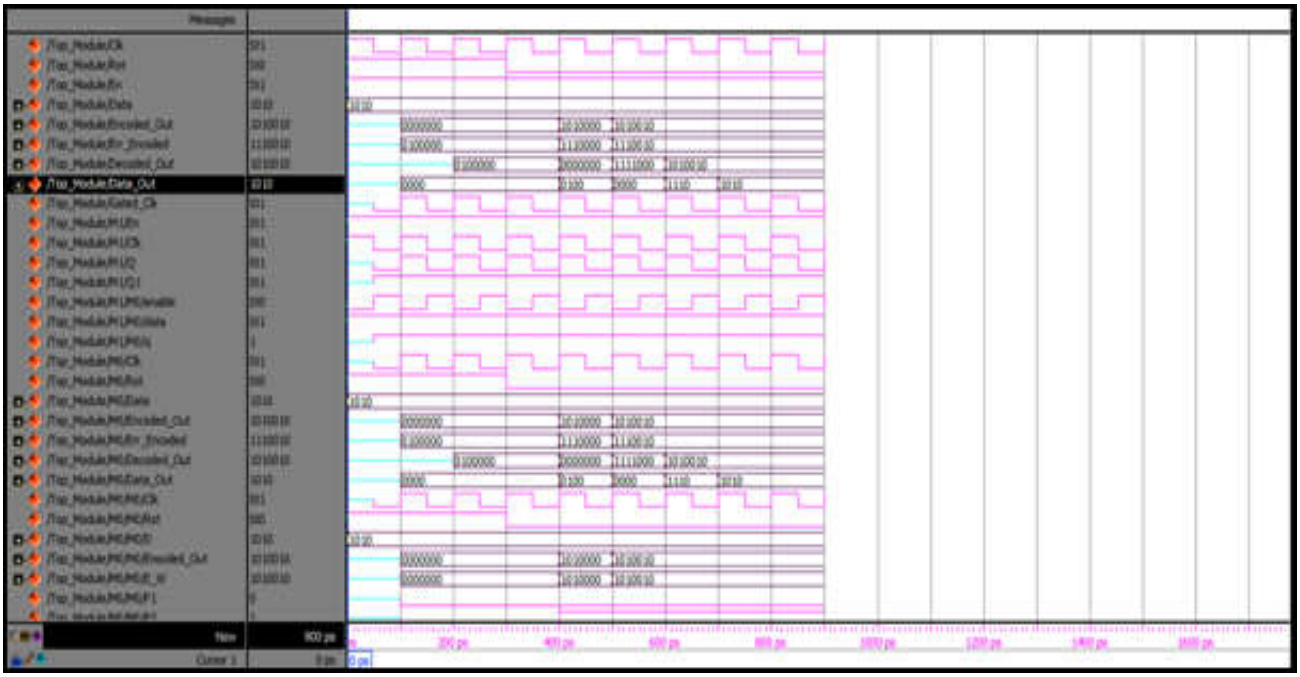
The clock -gating is one of the effective logic in RTL and architectural power reduction.

Clock gating is an effective technique to reduce dynamic power, because individual IP usage varies across applications, not all IP cores are used all the time, giving rise to opportunity for reducing the unused IP cores' power. By combining(AND gate) the clock with a gate-control signal, clock gating essentially disables the clock to an IP core when that IP is not used, avoiding power dissipation due to unnecessary charging and discharging of the unused circuits. The clock -gating is one of the effective logic in RTL and architectural power reduction. Clock gating is an effective technique to reduce dynamic power.

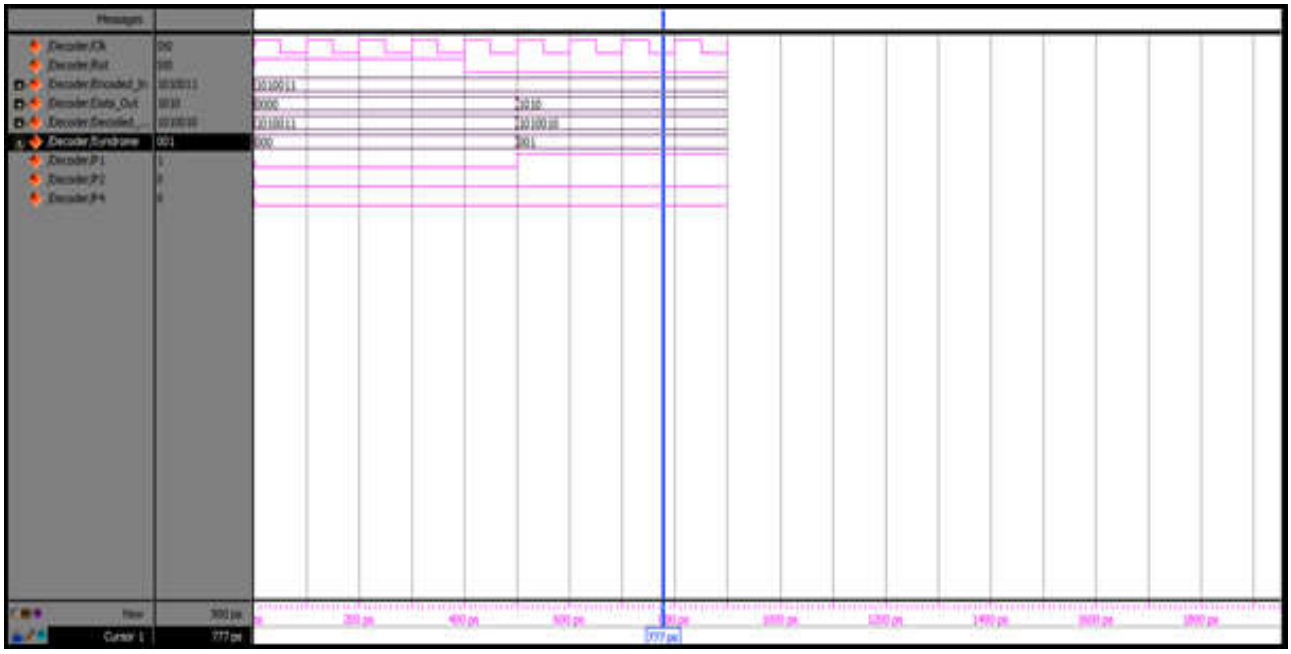


## V. SIMULATION RESULTS

Main Clock gating

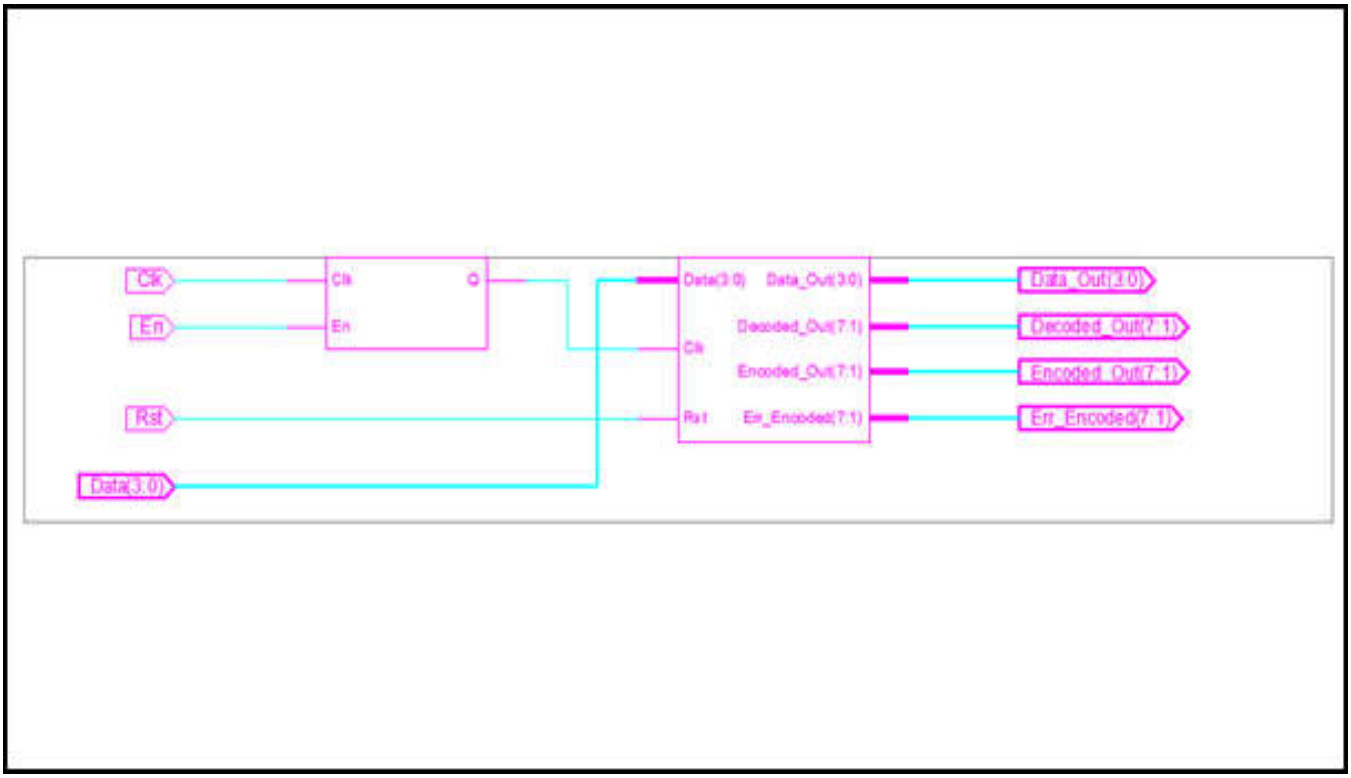


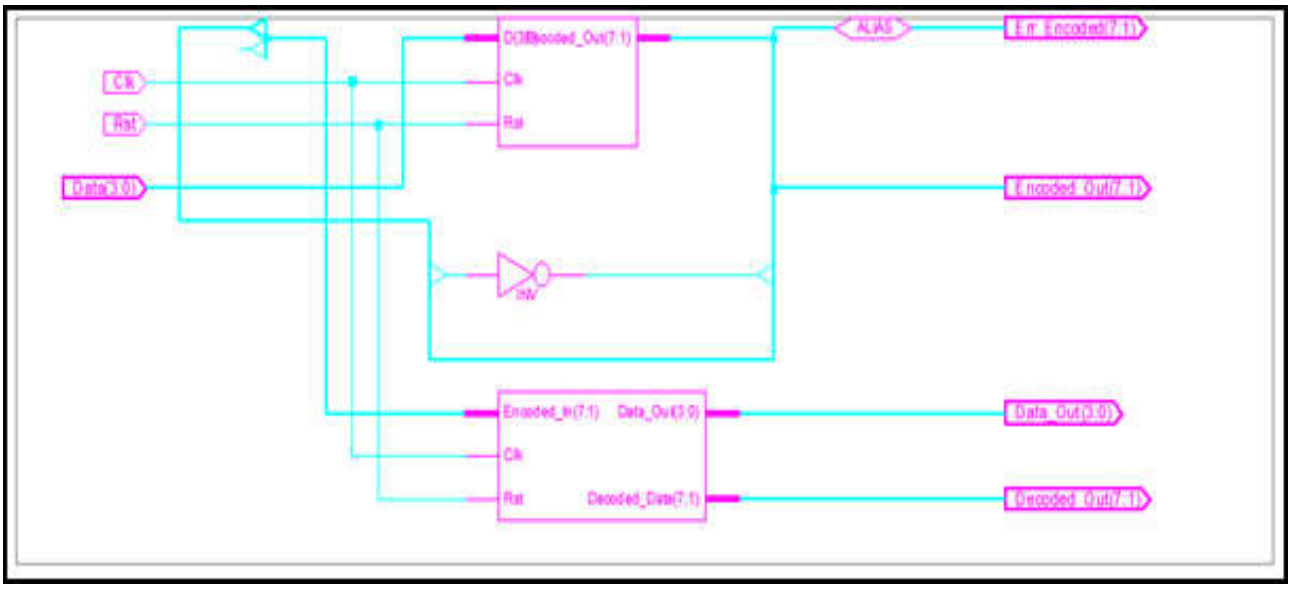
Clock gating based Encoder



Clock gating based Decoder

Encoder and with single bit Error Correction



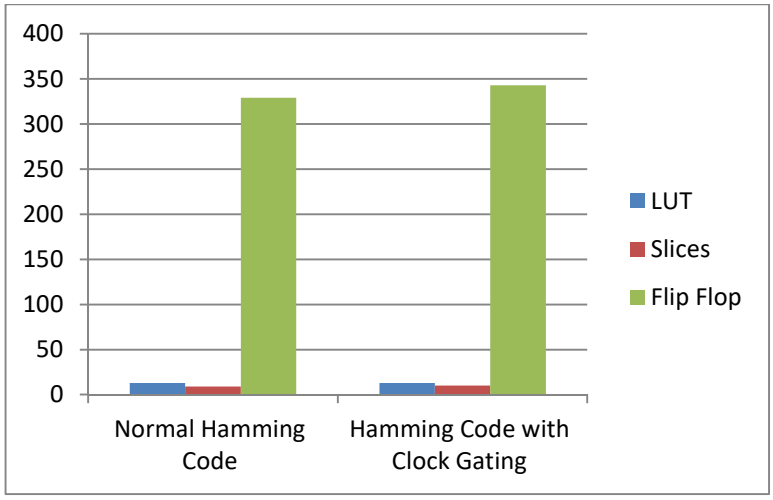



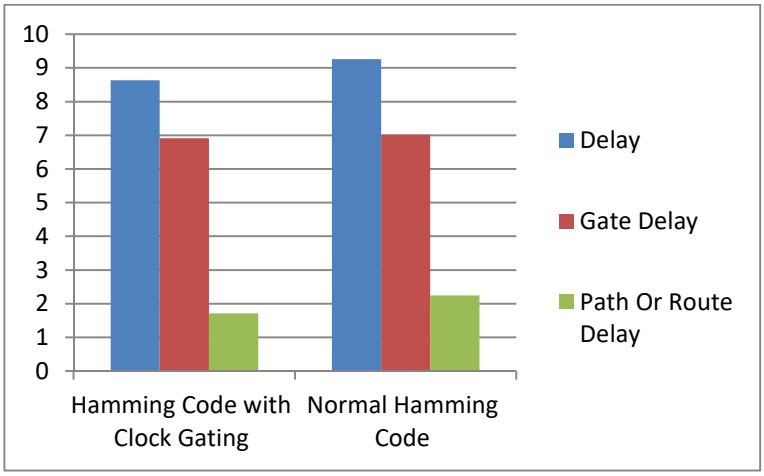

**HAMMING DESIGN RTL DESIGN**

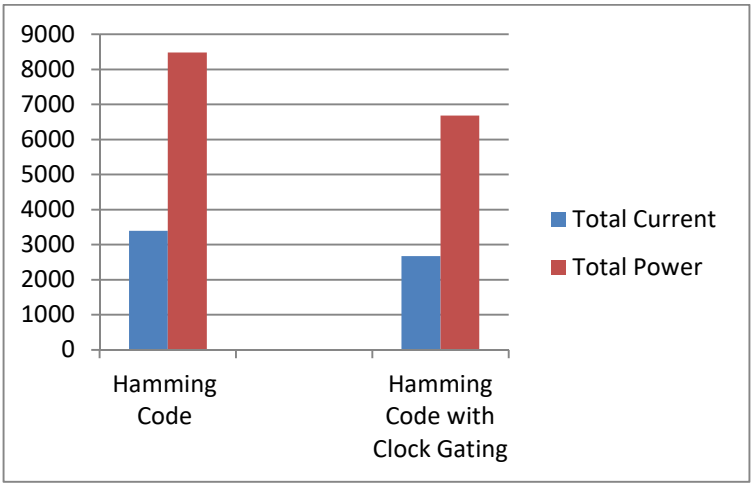
## VI. COMPARISON AND ANALYSIS

The Proposed Encoder and decoder designs are implemented using Verilog HDL, synthesized using Xilinx for different bit sizes and the delay and area have been analyzed for comparison

| METHOD NAME | AREA IN NUMBER OF LUT | | | DELAY | | | POWER | |
|---|---|---|---|---|---|---|---|---|
| | LUT | SLICES | FLIP FLOP | DELAY | GATE OR LOGIC DELAY | PATH OR ROUTE DELAY | TOTAL CURRENT (mA) | TOTAL POWER (mW) |
| Normal | 3 | 2 | 2 | 9.265 ns | 7.0165 ns | 1.4 249 ns | 3391.4 86 | 8481.4 14 |
| Hamming Code | 13 | 9 | 329 | 8.633 ns | 6.915 ns | 1.718 ns | | |
| Hamming Code with Clock Gating | 13 | 10 | 343 | 8.633 ns | 6.915 ns | 1.718 ns | 2671 | 6679.69 |






## VII. CONCLUSION

This paper provides an innovative approach to reduce power consumption in hamming code circuitry using clock gating logic gates. Proposed reversible Hamming Code encoding and decoding circuit equal number of gates and better power consumption. Proposed clock gating provide better Performance in Power. This encoder & decoder is implemented by FPGA Spartan 3.

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